GERÊNCIA DE ESPECIALISTAS EM SISTEMAS ELÉTRICOS DE POTÊNCIA

LABORATÓRIO DE ELETRÔNICA DE POTÊNCIA, ACIONAMENTOS E CONTROLE DE PROCESSOS INDUSTRIAIS

MMC AND CHB CONVERTER BOARD DESIGN REPORT

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CONTENTS

1. REPORT VERSION CONTROL

Responsible	Reason	Date
Dayane, Renata, Diogo e Jonathan	First Version	11/02/2020
Allan Fagner Cupertino	Review of the design methodology and format	26/03/2020
Renata Sousa	Thermal Design (semiconductor device selection)	31/03/2020
Renata Sousa	Inclusion of last PCB improvements	10/12/2020
Renata Sousa	Inclusion of review	17/12/2020

2. INPUT PARAMETERS

This project considerers that submodules (SMs) could be employed is two distinct cascaded configurations: three-phasic cascaded H-bridge in delta-connection (Δ-CHB) and monophasic modular multilevel converter with half-bridge SMs (HB-MMC).

The input parameters of this project are presented in Table 1.

Table 1 - Minimum specifications of the inverter.

Parameter	Symbology	Specification
Arm/cluster current	$I_{st,rms}$	7 A (rms)
Grid voltage (Δ-CHB)	$V_{g,\Delta}$	220 V (line to line rms)
Grid voltage (HB-MMC – monophasic)	$V_{g,MMC}$	127 V (line to line rms)
Number of FB-SMs (Δ-CHB)	N_{Δ}	4 (per cluster)
Number of HB-SMs (HB-MMC – monophasic)	N_{MMC}	6 (per arm)

3. SEMICONDUCTOR DEVICES REQUIREMENTS

Considering the modulation with injection of third harmonic, the minimum required dc-link can be approximated by (30 % of margin to include voltage drop in inductors, grid voltage variation, deadtime and current dynamics):

$$V_{dc,min,\Delta} \approx 1.3 \times \hat{V}_{g,\Delta} = 1.3 \times \sqrt{2} \times 220 = 404.46\,V \approx 400V. \quad (1)$$

$$V_{dc,min,MMC} \approx 2 \times 1.3 \times \hat{V}_{g,MMC} = 2 \times 1.3 \times \sqrt{2} \times 127 = 466{,}97\,V \approx 470V, \quad (2)$$

where $\hat{V}_{g,MMC}$ and $\hat{V}_{g,\Delta}$ are the grid voltage peak values.

In such conditions, the maximum voltage per SM is given by (10 % of ripple and 10 % of overshoot → 20 % of margin):

$$V_{sm,max,\Delta} = 1.2 \times \frac{V_{dc,min,\Delta}}{N_Y} = 1.2 \times \frac{400}{4} \approx 120\,V, \quad (3)$$

$$V_{sm,max,MMC} = 1.2 \times \frac{V_{dc,min,MMC}}{N_{MMC}} = 1.2 \times \frac{470}{6} \approx 94\,V. \quad (4)$$

Considering a utilization factor (f_u) of the semiconductor devices of 60 %, the minimum voltage class for each case is given by:

$$V_{std,\Delta} = \frac{V_{sm,max,\Delta}}{f_u} = \frac{120}{0.6} \approx 200\,V. \quad (5)$$

$$V_{std,MMC} = \frac{V_{sm,max,MMC}}{f_u} = \frac{94}{0.6} \approx 156.67\,V, \quad (6)$$

In the design, semiconductor devices with blocking voltage higher than 600 V are considered. Under such conditions, the dc-link voltage can be increased until 450 V. This fact can be useful to validate fault tolerance strategies (increase the arm voltage). Furthermore, the full bridge can be used in other projects for PV applications. In addition, for voltage rating higher than 600V there are IGBT commercially available. Moreover, to guarantee this applicability, the thermal design considers a switching frequency of 20 kHz.

The peak of cluster/arm currents is computed to help in the IGBT pre-selection. Thus, considering Table 1, the peak current in each cluster/arm is given by:

$$\hat{I}_{st} = \sqrt{2} I_{st,rms} = \sqrt{2} \times 7 \approx 10\,A. \quad (7)$$

In order to increase the range of operation safety IGBTs part numbers with current rating higher than 15 A are taken into account.

4. SEMICONDUCTOR DEVICES THERMAL DESIGN

4.1 Semiconductor Device Selection

Following the conclusions and considerations of last section, the semiconductor devices realization possibilities are investigated. Therefore, it is considered semiconductor voltage class higher than 600V and forward current in range of 15 A to 30A, in which 20 kHz switching frequency is supported.

Discrete devices are chosen, due to the facility of maintenance. In addition, Silicon IGBT of Infineon manufacturer are investigated due to the facility of test of these technologies on the manufacturer web site [1]. Moreover, package TO-220 and TO-247 are prioritized. Table 2 presents IGBT Infineon possibilities which fulfil these considerations.

Each Discrete IGBT is simulated in the manufacturer website [1] [2]. The simulation is realized in PLECS environment, as presented on the schematic of Figure 1. This simulation model includes thermal evaluation. For this reason, the power losses and junction temperature are evaluated by this simulation. In the analyses, it is considered grid frequency of 60 Hz, grid voltage of 220 V and grid current of 10 A. It is considered null thermal resistance (case to reference) and reference temperature of 80ºC, in order to simulate case temperature of 80ºC.

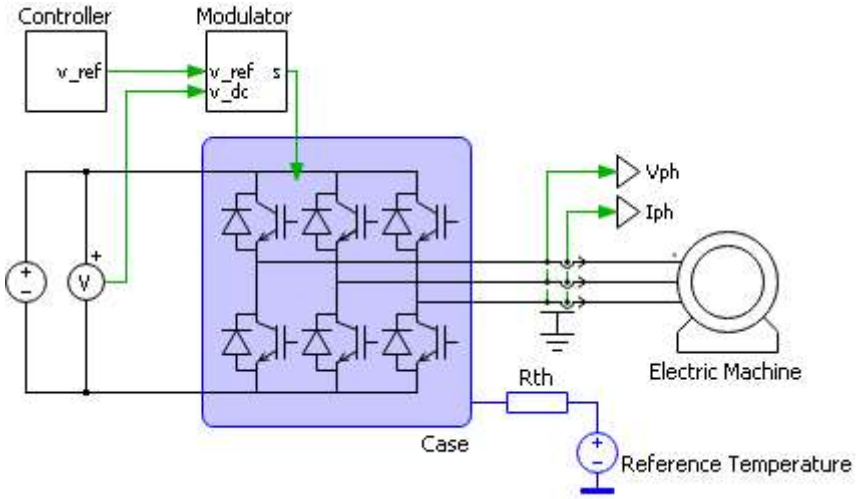


Figure 1 - Discrete IGBT Motor Drive Schematic [1].

Table 2 presents the power losses with different power factors (FP). The FP = 0 represents the reactive power operation (STATCOM) and FP = 1 the active power operation (HVDC). For the IGBTs evaluated, the junction temperature is lower than 116ºC. AS observed in Table 2, the IGBT part number IKP20N60H3 presents the better tradeoff between power losses and unitary cost in both operation conditions. Therefore, this IGBT is considered in this project.

Table 2 – IGBT Infineon Evaluation [1] [2].

Part Number	Voltage Class (V)	Ic @100°C (A)	Power Losses (W) FP = 0	Power Losses (W) FP = 1	Price per unit		Distributor
					10 units	100 units	
IKP10N60T	600	18	14,290	14,381	$1.68	$1.27	Infineon
IKP15N60T	600	23	12,997	12,782	$2.21	$1.62	Digi-key
IKP15N65H5	650	18	10,664	10,597	$2.11	$1.65	Infineon
IKP20N60H3	**600**	**20**	**10,575**	**10,603**	**$2.28**	**$1.68**	**Digi-key**
IKP20N60T	600	28	12,54	12,276	$2.51	$1.90	Infineon
IKP20N65F5	650	21	10,135	10,040	$2.39	$1.86	Infineon
IKP20N65H5	650	21	10,403	10,368	$2.38	$1.81	Infineon
IKW20N60H3	600	20	10,575	10,603	$2.80	$2.24	Infineon
IKW20N60T	600	28	12,540	12,276	$3.12	$2.50	Infineon
IKW30N60H3	600	30	11,294	11,208	$3.39	$2.56	Infineon
IRGB4062D	600	24	11,712	11,746	$4.3	$3.25	Infineon
IRGB4620D	600	20	11,942	11,536	$2.79	$2.10	Infineon
IRGB4630D	600	30	12,899	12,644	$3.61	$2.89	Infineon
IRGP4062D	600	24	11,716	11,752	$5.21	$4.17	Infineon

* FP = Power Factor.

4.2 Heatsink Selection

In order to select the heatsink, the maximum thermal impedance surface to ambient is computed, as follows:

$$R_{sA,max} = \frac{T_C - T_A}{P_{dissipated}} - R_{cA} \tag{8}$$

where T_C is the maximum case temperature in °C of the device as indicated by manufacturer. T_C = 80 °C is considered in this design. Moreover, T_A is the ambient temperature in °C. The rise in temperature caused by radiant heat of the heatsink should be increased by a margin of 10-30 °C. In this design, $T_A = 40$ °C is considered. $P_{dissipated}$ is the maximum power rating of device in Watts and R_{cA} is thermal resistance of mounting surface.

According to [3], the approximate values of Table 3 are employed.

Table 3 - Thermal resistance of mounting surface [3].

Material	Resistance (K/W)
Dry, without insulator	0.05 – 0.20 K/W
With thermal compound/without insulator	0.005 – 0.10 K/W
Aluminium oxide wafer with thermal compound	0.20 – 0.60 K/W
Mica wafer (0.05 mm thick) with thermal compound	0.40 – 0.90 K/W

For this project, the mica wafer is used. Thus, the resistance employed is R_{cA} = 0.40 K/W. Therefore,

$$R_{sA,max} = \frac{T_C - T_A}{P_{dissipated}} - R_{cA} = \frac{80°C - 40°C}{4.5\ W} - 0.4\ \frac{°C}{W} \approx 8.49\ \frac{°C}{W} \tag{9}$$

The heatsink choose should considered how it is represented in the manufacturer's catalog. According to the manufacturer chosen for this project, all of its models had a temperature of 75°C and a length of 4 inches. In this way, it is necessary to carry out conversions to adapt to the catalog model.

Table 4 - Variation of thermal resistance with temperature difference [4].

Δ°C	75	70	60	50	40	30
Correction factor	1.000	1.017	1.057	1.106	1.170	1.257

Considering the temperature correction factor of $\Delta = 40$ °C, gives:

$$R_{sA,max}(75℃) = \frac{2.74℃/W}{1.17} \approx 7.26 \frac{℃}{W} \quad (10)$$

Table 5 - Correction of thermal resistance for other heatsink lengths [4].

Length (mm)	10	20	30	40	50	70	100	150	200	250	300	400	500
correction factor	3.05	2.21	1.82	1.59	1.43	1.22	1.04	0.86	0.75	0.67	0.62	0.54	0.49

Using the length correction factor to 40 mm, given by:

$$R_{sA,max}(4") = \frac{7.26℃/W}{1.59} \approx 4.57 \frac{℃}{W} \quad (11)$$

According to the calculations above, the chosen model selected HS4225 [1].

4.3 Maximum Current and Switching Frequency

The system was simulated with different switching frequency and the maximum output current which respect the maximum junction temperature of the IGBT selected, in order to define the maximum SM operation condition.

The IGBTs were evaluated in half-bridge and full-bridge configuration, as illustrated in Figure 2 and Figure 3, respectively.

[1] https://www.hsdissipadores.com.br/catalogo.pdf

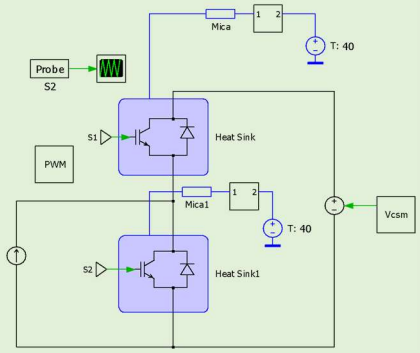


Figure 2- Half-bridge simulation.

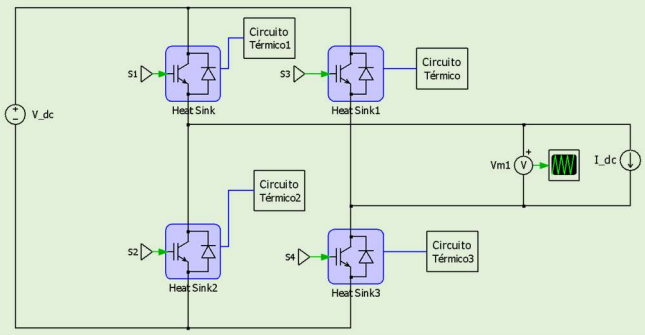


Figure 3 - Full-bridge simulation.

The design was tested considering different switching frequencies of each configuration, for a maximum junction temperature of 120º C, as show in Table 6 and Table 7 for half-bridge and full bridge configurations respectively. Tests were also made for the case of the full bridge circuit with only the AC component, for different power factors. The results are being shown in Figure 6.

Table 6 - Maximum output current with different PWM switching frequency for half-bridge configuration.

Frequency (kHz)	Max. Output Current RMS (A)
0.5	13,50
1	13,40
2	13,10
3	12,75
4	12,50
5	12,25
10	11,20
15	10,40
20	9,70

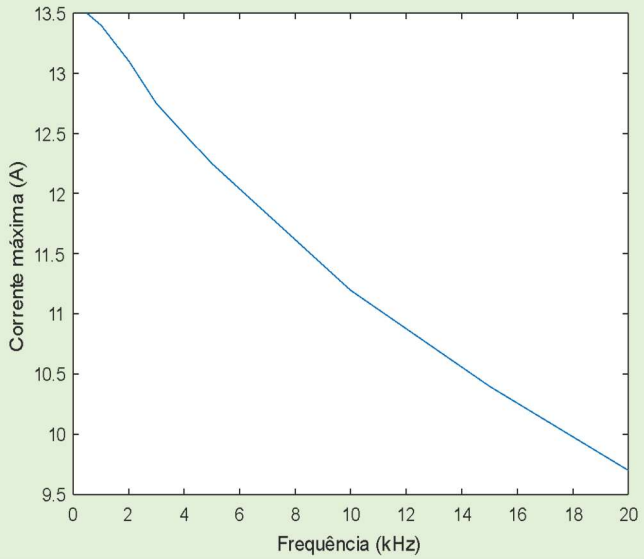


Figure 4 – Maximum output current as function of PWM switching frequency.

Table 7 - Maximum output current with different PWM switching frequency for full-bridge configuration.

Frequency (kHz)	Max. Output Current RMS (A)
0.5	13,50
1	13,40
2	13,00

3	12,75
4	12,50
5	12,25
10	11,20
15	10,40
20	9,65

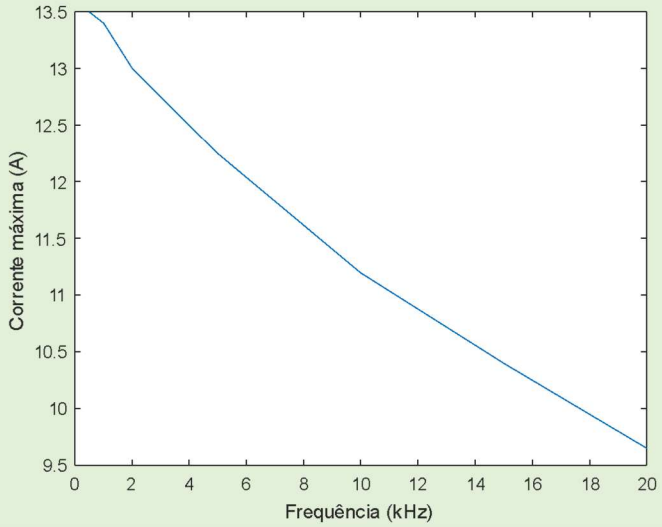


Figure 5 – Maximum output current as function of PWM switching frequency.

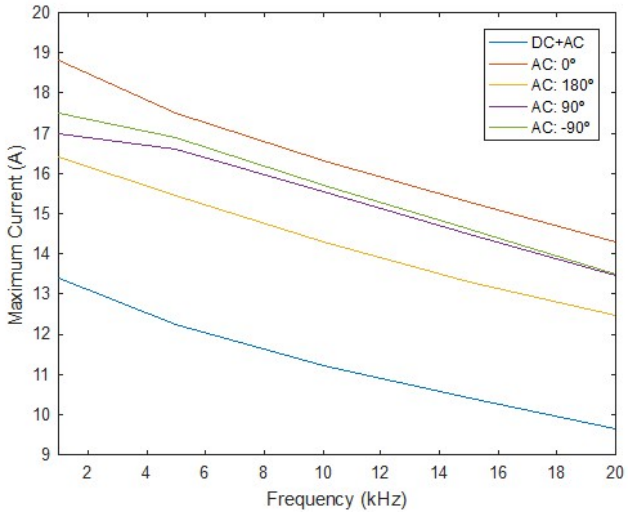


Figure 6 - Maximum output current as function of PWM switching frequency for different current components

5. SM CAPACITOR DESIGN

For this design, the nominal total power of the converters is given by:

$$S_{n,MMC} = I_g V_g = 2 I_{st,rms} V_g = 2 \times 7 \times 127 \approx 1.778\ kVA, \tag{12}$$

$$S_{n,\Delta} = \sqrt{3} I_g V_g = 3 I_{st,rms} V_g = 3 \times 7 \times 220 \approx 4.62\ kVA. \tag{13}$$

In addition, the maximum capacitor voltage is given by:

$$V_{sm,max,\Delta} = 1.2 \times \frac{V_{dc,min,\Delta}}{N_\Delta} \times K = 1.2 \times \frac{400}{4} \times \frac{4}{3} \approx 160\ V, \tag{14}$$

$$V_{sm,max,MMC} = 1.2 \times \frac{V_{dc,min,MMC}}{N_{MMC}} \times K = 1.2 \times \frac{470}{6} \times \frac{4}{3} \approx 125.33\ V, \tag{15}$$

where K is the voltage increase during redundant operation (1 failure for Δ-CHB and 2 failures for MMC). For this reason, capacitor with voltage higher than 160 V are considered.

Moreover, the maximum rms ripple current in the capacitor can be approximated by [5]:

$$I_{cap,rms,\Delta} = \frac{\hat{I}_g}{3}\sqrt{\frac{2}{\pi}} = \frac{7 \cdot \sqrt{3}\sqrt{2}}{3}\sqrt{\frac{2}{\pi}} \rightarrow I_{cap,rms,\Delta} = 4.56\ A \tag{16}$$

$$I_{cap,rms,MMC} = \frac{\hat{I}_g}{4} = \frac{7 \cdot 2\sqrt{2}}{4} \rightarrow I_{cap,rms,MMC} = 4.94 A \tag{17}$$

5.1 SM capacitance based on energy storage requirements

It is considered a ripple of 10 % and sinusoidal modulation. For the cases of MMC the minimum energy storage requirement considered is 60 J/kVA, while for Δ−CHB the minimum energy storage requirement is 30 J/kVA.

The total required energy storage is given by:

$$E_{nom,MMC} = W_n \times S_n = 60 J/kVA \times 1.778\ kVA = 106.68\ J, \tag{18}$$

$$E_{nom,\Delta} = W_n \times S_n = 30\ J/kVA \times 4.62\ kVA = 138.6\ J\ . \tag{19}$$

Therefore, the cell capacitance is given by:

$$C_{MMC} \geq \frac{2\ E_{nom}}{2N\ V_{sm,MMC}^2} = \frac{2 \times 106.68}{2 \times 6 \times \left(\frac{470}{6}\right)^2} \rightarrow C \geq\ 2.90\ mF\ , \tag{20}$$

$$C_\Delta \geq \frac{2\ E_{nom}}{3N\ V_{sm,\Delta}^2} = \frac{2 \times 138.6}{3 \times 4 \times \left(\frac{400}{4}\right)^2} \rightarrow C \geq\ 2.31\ mF. \tag{21}$$

The SM voltage ripple estimated in this design is [5]:

$$\delta_{MMC} = \frac{5S_{n,MMC}}{24\omega\hat{V}_{g,MMC}V^*_{sm,MMC}C_{MMC}} = \frac{5 \times 1.778\ kVA}{24 \times 2\pi 60 \times 127\sqrt{2}\left(\frac{470V}{6}\right) \times 2.9mF} \tag{22}$$

$$\delta_{MMC} = 2.41\% \ (\approx 1.89V)$$

$$\delta_{\Delta} = \frac{S_{n\Delta}}{6\sqrt{3}\omega\hat{V}_{g,\Delta}V^*_{sm,\Delta}C_{\Delta}} = \frac{4.62\ kVA}{6\sqrt{3} \times 2\pi 60Hz \times \frac{220V}{\sqrt{3}}\sqrt{2}\left(\frac{400V}{4}\right) \times 2.31mF} \tag{23}$$

$$\delta_{\Delta} = 2.84\% \ (\approx 2.84V)$$

This ripple is very low for the analyses desired in future experimental results.

5.2 SM capacitance based on Ripple realization

SM voltage ripple of $\delta_{MMC} = 10\%$ is considered. Thus [5],

$$C_{MMC} = \frac{5S_{n,MMC}}{24\omega\hat{V}_{g,MMC}V^*_{sm,MMC}\delta_{MMC}} = \frac{5 \times 1.778\ kVA}{24 \times 2\pi 60 \times 127\sqrt{2}\left(\frac{470V}{6}\right) \times 0{,}1} \tag{24}$$

$$C_{MMC} = 0{,}698mF$$

$$C_{\Delta} = \frac{S_{n\Delta}}{6\sqrt{3}\omega\hat{V}_{g,\Delta}V^*_{sm,\Delta}\delta_{\Delta}} = \frac{4.62\ kVA}{6\sqrt{3} \times 2\pi 60Hz \times \frac{220V}{\sqrt{3}}\sqrt{2}\left(\frac{400V}{4}\right) \times 0{,}1} \tag{25}$$

$$C_{\Delta} = 0{,}656mF$$

The realization of this capacitance is made by 1 capacitor manufacturer EPCOS - TDK Electronics of 680µF 200V Aluminum Electrolytic Capacitors Radial, part number B43634A2687M060. This capacitor supports ripple current of 4.63A @100Hz at 60°C.

The capacitor chosen also provide the possibility to employ 4 capacitors in parallel for supply the design of the previous subsection.

6. BLEED RESISTOR DESIGN

Considering the 1 capacitor of 680µF in each SM for the topologies MMC and Δ−CHB, it is possible to calculate the bleed resistor considering converter power losses equal 0.5%.

For MMC, the power losses per SM are:

$$S_{n,MMC} \times \frac{0.5}{100} = 1.778kVA \times \frac{0.5}{100} = 8.89W = P_{MMC} \times N_{MMC} \times 2 \quad (26)$$

$$P_{MMC} = 0.74W \quad (27)$$

Considering these losses, the bleeding resistance is:

$$P_{MMC} = \frac{V^2}{R_{b,MMC}} \Rightarrow R_{b,MMC} = \frac{V^2}{P_{MMC}} = \frac{200^2}{0.74} = 54.05k\Omega \quad (28)$$

For Δ−CHB, the power losses per SM are:

$$S_{n,\Delta} \times \frac{0.5}{100} = 4.62\ kVA \times \frac{0.5}{100} = 23.1W = P_{\Delta} \times N_{\Delta} \times 3 \quad (29)$$

$$P_{\Delta} = 1.93W \quad (30)$$

Considering these losses, the bleeding resistance is:

$$P_{\Delta} = \frac{V^2}{R_{b,MMC}} \Rightarrow R_{b,\Delta} = \frac{V^2}{P_{\Delta}} = \frac{200^2}{1.93} = 20.73k\Omega \quad (31)$$

Commercial Resistor

For MMC and Δ−CHB, the commercial resistors which fulfil the previous consideration are 56 kΩ / 1 W and 21 kΩ / 2 W, respectively. Nevertheless, in order to employ a unique type of bleeding resistor, the resistor of R_b = 56 kΩ / 1 W is chosen. The discharge with this resistor is given by:

$$5\tau = 5R_bC = 5 \times 56\ k\Omega\ \times 680\mu F = 190s = 3min10s \quad (32)$$

The power losses in both cases are:

$$P = \frac{V^2}{R_b} = \frac{200^2}{56 \times 10^3} = 0.71W \quad (33)$$

Percentage of losses for MMC:

$$\frac{P \times N_{MMC} \times 2}{S_{n,MMC}} = \frac{8.57W}{1.778kVA} = 0.48\%$$

Percentage of losses for Δ−CHB:

$$\frac{P \times N_{\Delta} \times 3}{S_{n,\Delta}} = \frac{8.57W}{4.62\ kVA} = 0.18\%$$

Therefore, R_b = 56 kΩ / 1 W is employed for both topologies.

Device suggestion: Metal Film Resistors 1watt 56Kohms 5%, part number PR01000105602JA100.

7. HIGH FREQUENCY CAPACITOR

This capacitor is employed to filter the high frequency instabilities of the SM. This capacitor must fulfil the voltage requirements of the SM. The capacitance stipulated is 1µF.

Therefore, a polyester EPCOS capacitor of 1µF/250V, part number B32522.

8. BYPASS STRUCTURE DESIGN

Two protection devices were implemented which can guarantee fast reaction times (TRIAC) and permanent SM by-pass with little losses (RELAY).

8.1 TRIAC

- A Triac is used for its ability to switch independent of the current direction;
- The Triac is controlled by an Opto-Triac;
- Since the maximum current output of the DSP is under 20mA and the LED in the opto-triac (MOC3041) requires at least 15mA, a transistor was used to control the LED.
- A pull-down resistor is used at the base of the transistor in order to ensure that it will not be turned on by Electro Magnetic Interferences (EMI).

For the SM bypass, the following TRIAC circuit is employed:

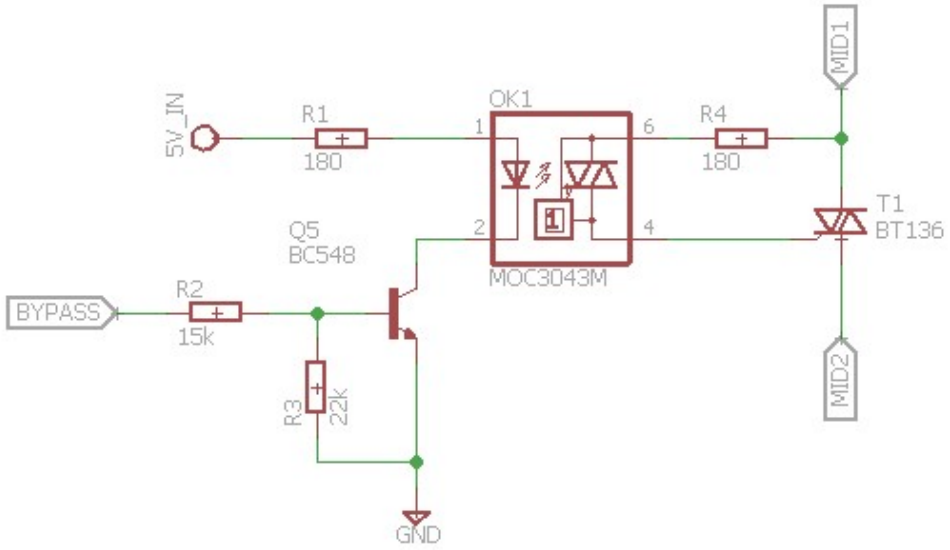


Figure 7 – Schematic of the bypass circuit (TRIAC representation).

Considering that the LED trigger current ($I_C = I_{LED}$) of triac driver photocoupler is 15 mA and the maximum absolute value is 60 mA, the resistor R_1 is evaluated to ensure $I_c = 20mA$. Thus:

$$R_1 = \frac{(V_{CC} - V_F - V_{CE})}{I_C} = \frac{5 - 1.3 - 0.2}{20 \times 10^{-3}} = 175\,\Omega\,, \tag{34}$$

The transistor BC548 is used to guarantee a current gain of $\beta = 110$. In this view, the base current is:

$$I_B = \frac{I_C}{\beta} = \frac{20 \times 10^{-3}}{110} = 0.18\,mA \tag{35}$$

Once the base current was calculated, the resistor R_2 can be given by:

$$R_2 = \frac{V_{DSP} - V_{BE}}{I_B} = \frac{3.3 - 0.6}{0.18 \times 10^{-3}} = 15\ k\Omega \quad (36)$$

The pull-down resistor is chosen based on typical values, in this work, $R_3 = 22\ k\Omega$. Moreover, the resistor R_4 is used to limit the gate current of TRIAC. According to [6], the surge current in the gate can reach half the peak gate current (I_{GM}). Thus, the resistor can be evaluated by:

$$R_4 \geq \frac{V_{sm,max}}{0.5 I_{GM}} = \frac{120\ V}{1\ A} = 120\ \Omega \quad (37)$$

8.2 RELAY

- An inrush current diode was placed in parallel to the relay, in order to protect the transistor from the high inrush current which will appear at the turn off of the relay.
- Since the relay needs a higher current on the control side to be driven, as in TRIAC design, a transistor was used;
- A pull-down resistor was used in order to ensure that the relay won't be accidentally turned on.

For the SM bypass, the following relay circuit is employed:

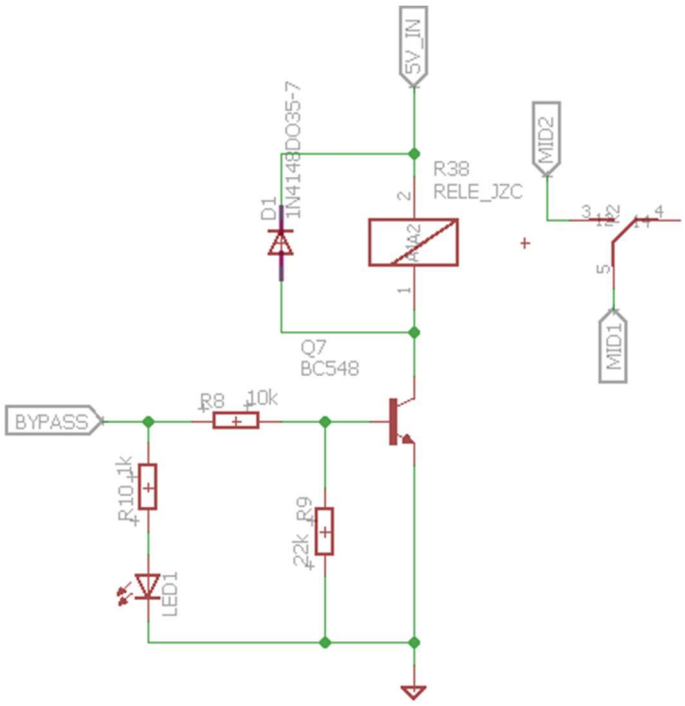


Figure 8 - Schematic of the bypass circuit (relay representation).

Considering that coil resistance of the relay (SRD-5VDC) is 70 Ω. The collector current can be evaluated by:

$$I_C = \frac{V_{CC} - V_{CE}}{R_{coil}} = \frac{5 - 0.2}{70} = 68.57\ mA \quad (38)$$

Therefore,

$$I_B = \frac{I_C}{\beta} = \frac{68.57 \times 10^{-3}}{110} = 0.62\ mA \tag{39}$$

The resistor R_8 is given by:

$$R_8 = \frac{(V_{CC} - V_{BE})}{I_B} = \frac{5 - 0.3}{0.62 \times 10^{-3}} = 7.58\ k\Omega\ , \tag{40}$$

As defined in TRIAC design, the pull-down resistor is chosen based on typical values, in this work, $R_9 = 22\ k\Omega$.

To indicate the bypass circuit operation, an LED with a current of $1.5\ mA$ is chosen. Thus, the LED resistor is given by:

$$R_{10} = \frac{V_{DSP} - V_{LED}}{I_{LED}} = \frac{3.3 - 1.9}{1.5 \times 10^{-3}} = 0.93\ k\Omega \tag{41}$$

Finally, based in commercial values, the main evaluated parameters are shown in Table 8.

Table 8 – Parameters used in the bypass circuit.

TRIAC						
R_1	R_2	R_3	R_4	*TBJ*	*TRIAC*	*Driver*
180 Ω	15 $k\Omega$	22 $k\Omega$	180 Ω	*BC548*	*BT139*	*MOC3041*
RELAY						
R_8	R_9	R_{10}	*Diode*	*Relay*	*LED*	
10 $k\Omega$	22 $k\Omega$	1 $k\Omega$	*1N4148*	*RELE_JZC − 36F 10A*	$3mm - 1.5mA$ (red)	

8.3 TRANSIENT PROTECTION

A varistor is also added to the circuit in order to protect against voltage transient. The voltage capability of this circuit is 220V.

Figure 9 - Varistor.

9. GATE DRIVER DESIGN

When choosing a gate driver, different aspects were taken into consideration: built-in insulation, half-bridge driving capability, easy dead-time implementation, driver disable function and possibility to be used in a bootstrap configuration.

The IR2104 Integrated Circuit (IC) from International Rectifier, was chosen based on its qualities. The floating channel is designed for bootstrap operation and can be used to drive an N-channel power MOSFET or IGBT in the high side configuration. It can support up to 500 V between driving outputs. As a general rule the local V_{CC} decoupler capacitor is $C_{VBP} = 100\ nF$.

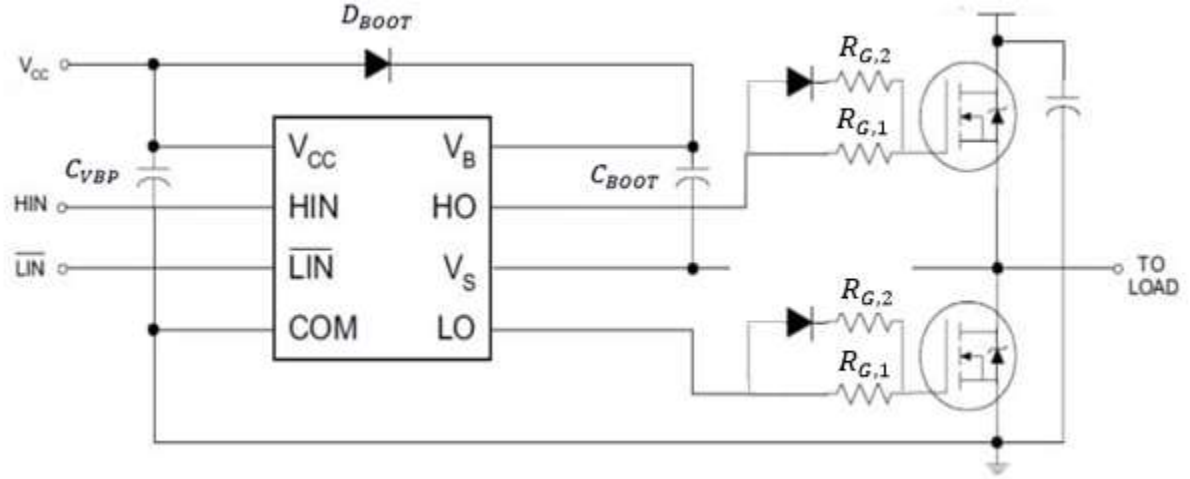


Figure 10 – Gate driver schematic (IR2104).

The calculations for the bootstrap circuit are done considering the switching frequency and the gate charge of the IGBT. Considering the IGBT switch IKP20N65F5, the total gate charge is $Q_G = 48\ nC$. Moreover, a maximum allowed voltage drop for the driving circuit selected is $\Delta V_{BOOT} = 0.2\ V$ [7]. The minimum bootstrap capacitor is calculated as:

$$C_{BOOT} = \frac{Q_G + I_{Q,BOOT}\frac{D_{max}}{f_{sw,min}}}{\Delta V_{BOOT}} = \frac{48 \times 10^{-9} + \left(10 \times 10^{-6}\frac{0.95}{20}\right)}{0.2} = 2.62\ \mu F\ , \quad (42)$$

where, $I_{Q,BOOT}$ is the quiescent current of the bootstrap circuit, D_{max} is the maximum duty cycle and $f_{sw,min}$ a minimum switching frequency. $I_{Q,BOOT} = 10\ \mu A$ is a typical value of bootstrap current. A maximum duty cycle of $D_{max} = 0.95$ is employed. Since the power converter can operate with electric drives, the minimum switching frequency chosen is $f_{sw,min} = 20\ Hz$.

The rule of thumb is to select a good quality ceramic capacitor with some reserve, usually double the size is a good practice. For this circuit the bootstrap capacitor is a $4.7\ uF$ ceramic capacitor.

A Schottky diode is generally recommended as the bootstrap diode. For this, the average forward current for selecting the diode can be estimated based on a maximum switching frequency of $20\ kHz$ as:

$$I_F = Q_G \times f_{sw,max} = (48 \times 10^{-9}) \times (16 \times 10^{3}) = 0.960\ mA\,, \tag{43}$$

The driving circuit needs to load the IGBT gate charge in order to open it, and most of the times a gate resistance needs to be present in order to limit the current. The resistance can be calculated based on the gate charge, the turn-on delay time and turn-on rise time. The equation for the gate current is computed by:

$$I_G = \frac{Q_G}{t_{d(on)} + t_r} = \frac{48 \times 10^{-9}}{19 \times 10^{-9} + 13 \times 10^{-9}} = 1.5\ A\,, \tag{44}$$

After this, considering the supply voltage (V_{CC}) and the nominal current gate voltage ($V_{GS,I}$), the on gate resistance can be calculated by [8]:

$$R_{G,on} = \frac{V_{CC} - V_{GE(th)}}{I_G} = \frac{15 - 4.8}{1.5} = 6.8\ \Omega\,, \tag{45}$$

Furthermore, if $dV_{out}/dt = 1\ V/ns$, the turn-off gate resistor is calculated as [8]:

$$R_{G,off} \leq \frac{V_{GE(th),min}}{C_{gd(off)} \frac{dV_{out}}{dt}} = \frac{3.2}{(5 \times 10^{-12}) \times 10^{9}} = 640\ \Omega\,, \tag{46}$$

where $C_{gd(off)}$ is the Miller effect capacitor, specified as reverse transfer capacitance C_{res} in the IGBT datasheet.

The gate resistance can be employed as shown in Figure 10. In this case, the $R_{G1} = R_{G,off}$ and $R_{G,on} = R_{G1}//R_{G2}$. Thus,

$$R_{G2} = \frac{R_{G1} R_{G,on}}{R_{G1} - R_{G,on}}, \tag{47}$$

According to [9], the value of an optimized gate resistor will be somewhere between the value indicated in the IGBT ($R_G = 32\ \Omega$). Moreover, in most applications, the turn-on gate resistor $R_{G,on}$ is smaller than the turn-off gate resistor $R_{G,off}$. Depending on the individual parameters, $R_{G,off}$ can be roughly twice the $R_{G,on}$ value. Therefore, the gate resistors can be evaluated by:

$$R_{G1} = R_{G,off}\,, \tag{48}$$

$$R_{G2} = R_{G1} = R_{G,off}. \quad (49)$$

Finally, based in commercial values and the margins in the evaluated values, the main evaluated parameters are shown in Table 9.

Table 9 – Parameters used in the gate driver (IR2104) circuit.

$R_{G,1}$	$R_{G,2}$	C_{BOOT}	C_{VBP}	$Diode$
$32\ \Omega$	$32\ \Omega$	$4.7\ \mu F$	$100\ nF$	$1N5817 - B$

10. CONNECTION OF GATE DRIVERS TO IGBT

In order to minimize stray inductance between the gate driver and IGBT module, the circuit of Figure 11 is recommended [10].

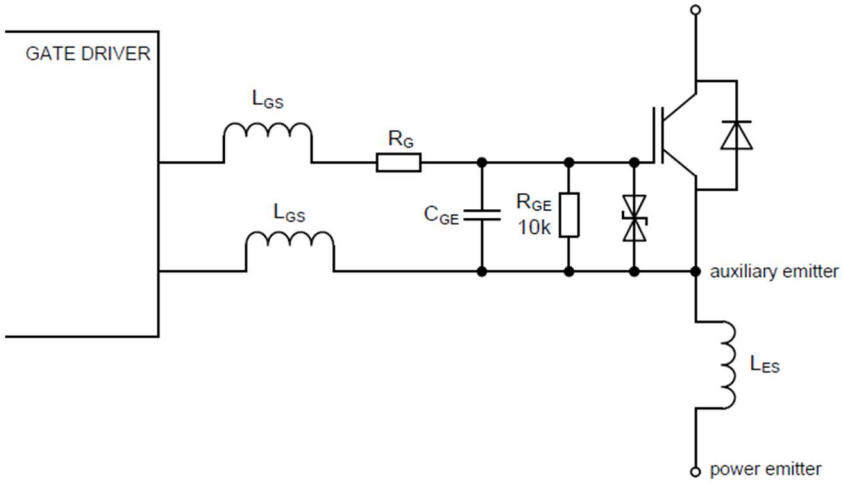


Figure 11 - Gate Driver Connection & Stray Inductances [10].

According to [10], it is recommended that a 10kΩ resistor (R_{GE}) be placed between the gate and emitter. If wire connection is used, do not place the R_{GE} between printed circuit board and IGBT module. R_{GE} has to be placed very close to the IGBT module.

Moreover, the use of a suppressor diode (back-to-back Zener diode) between gate and emitter is recommended. The diode has to be placed very close to the IGBT module. In this project, two Zener diodes of 15V Vishay, part number BZX584C15-G3-08, are employed.

Furthermore, the use of a capacitor (C_{GE}) between gate and emitter can be advantageous, even for high-power IGBT modules and parallel operation. The C_{GE} has to be placed very close to the IGBT module. The C_{GE} should be approximately 10% of the gate-emitter capacitance (C_{GE}*) of the IGBT used. Considering the IGBT IKP20N60H3 datasheet and reference [11], the C_{GE} is given by:

$$C_{GE} = \frac{1}{10} C_{GE}^{*} = \frac{C_{ies} - C_{res}}{10} = \frac{1100pF - 5pF}{10} = \frac{1068pF}{10} = 106.8pF \approx 110pF \quad (50)$$

where C_{ies} is the IGBT input capacitance and C_{res} is the IGBT reverse transfer capacitance.

Therefore, in this project, a capacitor Kemet of 110pF, 50V, part number C0603C111J5GACTU, is employed.

11. CAPACITOR VOLTAGE MEASUREMENT DESIGN

Avago Technologies HCPL-7520 linear optoisolator was used in this project [12]. This device has a linear transfer characteristic curve for the -200 mV to 200 mV input range, Figure 12. The input is differential, and the output is scaled to v_{ref}. The gain is $\frac{v_{ref}}{0.512}$. This single chip allows you to polarize the signal to $\frac{v_{ref}}{2}$, amplify and isolate it [13]. v_{ref} was set to 5 V.

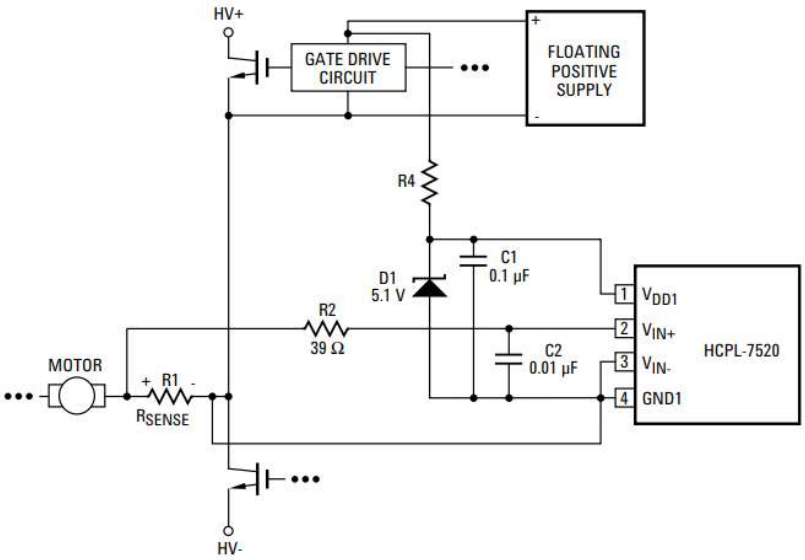


Figure 12 - Recommended supply and sense resistor connections [12].

To measure voltage, the idea is to use a very large voltage divider to divide the v_{system} = 250 V for MMC or v_{system} = 450 V for PV system down to level which can be sampled by the ADC, given by:

$$v_{in}^{+} = \frac{R_2}{R_1 + R_2} v_{system} \tag{51}$$

Performing the project for an MMC system the values of R_1 and R_2 are, respectively: 2.6MΩ and 2kΩ. Performing the project for a PV system the values of R_1 and R_2 are, respectively: 2.6MΩ and 1.1kΩ. By assigning the values obtained above it is possible to calculate the output voltage, v_{out}, of the IC [13].

$$v_{in}^{+} = \frac{0.512}{v_{ref}}\left(v_{out} - \frac{v_{ref}}{2}\right) \tag{52}$$

$$v_{out} = \frac{2v_{in}^{+}\, v_{ref} + v_{ref} \times 0.512}{2 \times 0.512} \tag{53}$$

Considering the MMC system, the output voltage of the HCPL-7520 will be equal to: v_{out} = 2.5 V (considering v_{in}=0V) and 4.45V (considering v_{in} =200mV).

In this way, the voltage obtained at the HCPL-7520 output exceeds the DSP power limit (3.3V). Thus, the solution adopted was to use TLV247X a subtractor-type operational amplifier to reduce this scale, Figure 13.

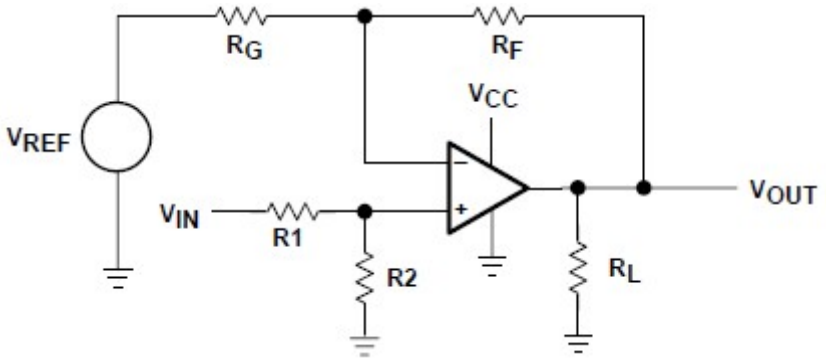


Figure 13 - Noninverting Op Amp [14].

Thus, when the output of the HCPL-7520 is equal to 2.5V, the output voltage of the op amp will be 0. For a voltage equal to 4.45V, the output of the op amp is approximately 3V, according to the equations below [15]:

$$v_{out} = (v_{cc} - v_{in})\frac{R_F}{R_G} \tag{54}$$

$$v_{out} = v_{in}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) - v_{ref}\frac{R_F}{R_G} \tag{55}$$

$$v_{out} = mv_{in} + b \tag{56}$$

$$\{0 = 2.5m + b\ 3 = 4.45m + b \tag{57}$$

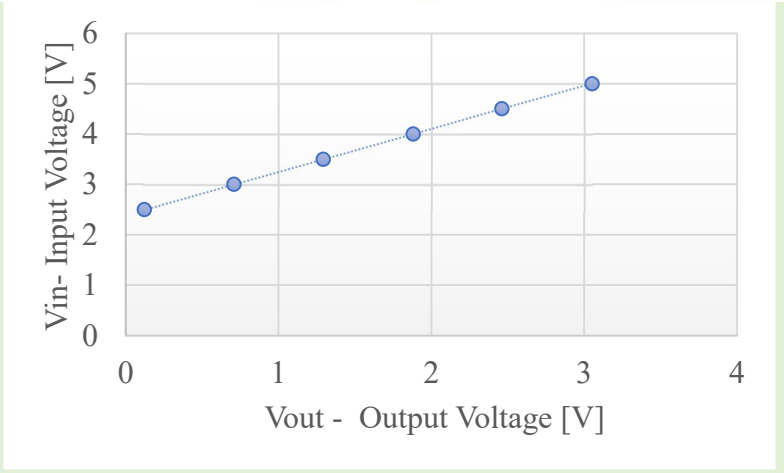
After determining the values of the gains $m = 1.539$ and $b = -3.846$, it is possible to calculate the values of the resistances to be used, given by.

$$b = -v_{ref}\left(\frac{R_F}{R_G}\right) \tag{58}$$

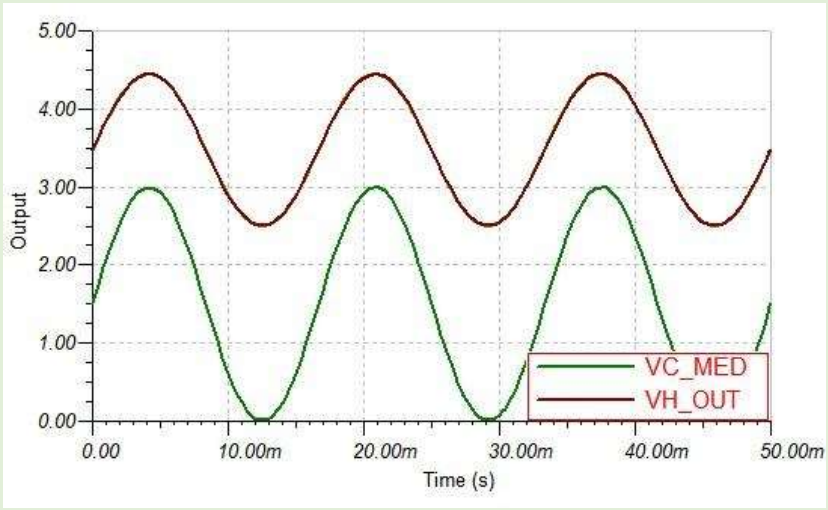
$$m = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{59}$$

The R_1 and R_G resistors were established at 7.68kΩ and 10kΩ, respectively. In this way, R_2 = 51.1kΩ (49.9kΩ), and R_F = 7.68kΩ. In addition, V_{CC} and V_{REF} = 5 V. After similar the circuit in the software TINA - Texas Instruments[2], the transfer curve for this circuit is shown in Figure 14.

[2] SPICE-based analog simulation program - TINA-TI - <http://www.ti.com/tool/TINA-TI >



(a)



(b)

Figure 14 - Circuit Measured Transfer Curve (*VC_MED and VH_OUT are the output and input of op-amp, respectively*).

12. POWER SUPLY PROTECTION

The main supply of the board is 5V. In order to protect the electronics from fluctuation of the external power supply, over-voltage or inversing polarity of the supply, the circuit in Figure 15 is employed.

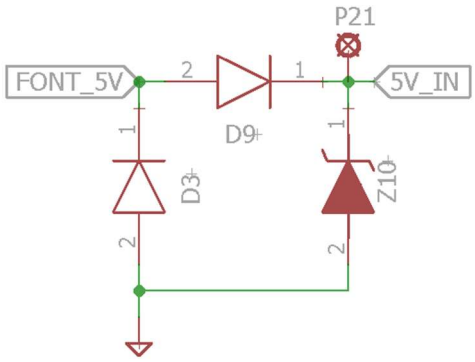


Figure 15 - Power supply protection.

In Figure 15, the Diode D3 is a fast recovery Schottky diode, rated for 30V and 3A, part number CMS01. It is placed there to ensure that if accidentally the polarity of the power supply is reversed, it will provide a conductive path and help protect the electronics on the board. Diode D9 is identical to D3 and its purpose is also to protect the board. In case of reverse polarity, it will block the reversed voltage and together with D3 will protect the components. Diode Z10 is an 5.6V Zener diode from Vishay, part number BZX384C5V6-HG3-08. In case the input voltage will be higher than 5.6V it will clamp it, and protect the voltage regulator from overheating due to the increased voltage.

13. ISOLATED POWER SUPPLY DESIGN

It is defined 5V as input voltage of the power supply system. Table 10 presents the components which require power supply with the respective voltage level.

Table 10 - Components power supply.

Component	Part Number	Voltage supply	Reference	Current supply
Input Buffers	SN74LV1T34	5 V	DSP	4 x 50 mA
Optocoupler	ACSL-6400	5 V	Full-bridge SM	10 mA
IGBT Gate drivers	IR2110	15V	Full-bridge SM	2 x 0.34 mA
Isolated Linear Sensing IC	HCPL-7520	5V	Full-bridge SM / DSP	2 x 16 mA
Bypass circuit	TRIAC+Rele+LED	15V	Full-bridge SM	2 mA

Considering the voltage levels above, 2 isolated dc/dc converters will be required according to Table 11.

Table 11 - dc/dc converters

dc/dc converter	Part Number	Output Current	Comments
5V/5V	TBA 1-0511	200 mA	https://assets.tracopower.com/20200326110658/TBA1/documents/tba1-datasheet.pdf
5/15V	TBA 2-0513	130 mA	https://assets.tracopower.com/20200326110658/TBA2/documents/tba2-datasheet.pdf

14. PCB PINOUT

The description of each pin of the Header connector of 14 pins is detailed in Table 12.

Table 12- Connector Header 14 pins.

Pin	Input or output (I/O)	Signal	Pin	Input or output (I/O)	Signal
14	I	GND_DSP	13	I	BYPASS
12	I	GND_DSP	11	I	GND_DSP
10	I	GND_DSP	9	I	PWM1
8	I	GND_DSP	7	I	GND_DSP
6	I	GND_DSP	5	I	RESET
4	I	GND_DSP	3	I	GND_DSP
2	I	GND_DSP	1	I	PWM2

The power supply connector MSTBA3 is detailed in Table 13.

Table 13 - Power supply connector MSTBA3.

Pin	Input or output (I/O)	Signal
1	I	5V
2	I	GND_DSP
3	I	Board Grounding

The SM voltage measurement connector MSTBA2 is detailed in Table 14.

Table 14 – SM Voltage measurement connector MSTBA2 (MED).

Pin	Input or output (I/O)	Signal
1	O	GND_DSP
2	O	VC_MED

The connector of the points between superior and inferior IGBTs, called as MID1 and MID2, are detailed in Table 15 and Table 16, respectively.

Table 15 – MID1 connector MSTBA2 (MID1).

Pin	Input or output (I/O)	Signal
1	O	MID1
2	O	MID1

Table 16 – MID2 connector MSTBA2 (MID2).

Pin	Input or output (I/O)	Signal
1	O	MID2
2	O	MID2

The connector of the SM voltage, called as V_CAP is detailed in Table 17.

Table 17 – SM voltage connector MSTBA2 (V_CAP).

Pin	Input or output (I/O)	Signal
1	O	V_CAP

2	O	V_CAP

The connector of the SM reference, called as GND_CELL is detailed in Table 18.

Table 18 – SM reference connector MSTBA2 (GND_CELL).

Pin	Input or output (I/O)	Signal
1	O	GND_CELL
2	O	GND_CELL

15. ASSEMBLED SUBMODULES

Five submodules of the first version were made and 10 more are being manufactured. Figure 16 shows the top view of the finished submodule of the first version

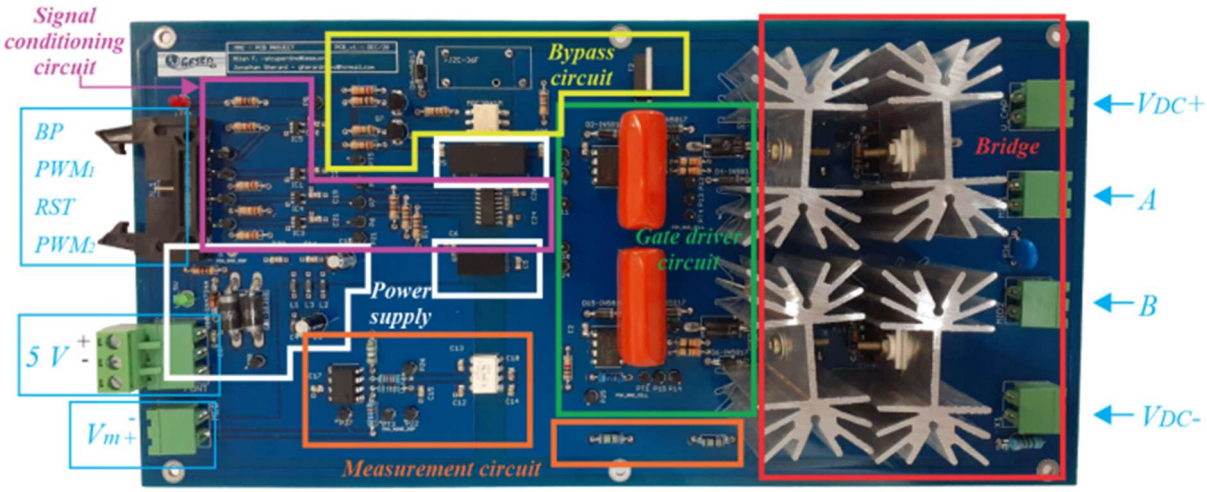


Figure 16 -Board top view.

16. REFERENCES

[1] "Discrete IGBT Motor Drive Simulator," Infineon, [Online]. Available: https://plex.infineon.com/plexim/igbtmotor.html?_ga=2.237241731.2085572244.1585569292-774482458.1584963065. [Accessed 27 Março 2020].

[2] "Discrete IGBT with Anti-Parallel Diode," Infineon, [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-discretes/discrete-igbt-with-anti-parallel-diode/. [Accessed 27 Março 2020].

[3] Fischer Elektronik, "SK9-XX-AL Datasheet," 2012.

[4] Hs Dissipadores, "Catálogo Hs Dissipadores," [Online]. Available: https://www.hsdissipadores.com.br/catalogo.pdf. [Accessed 29 March 2020].

[5] D. C. Mendonça, R. O. d. Sousa, J. V. M. Farias, H. A. Pereira, S. I. S. Jr and A. F. Cupertino, "Multilevel Converter for Static Synchronous Compensators: State-of-art, Applications and Trends".," in *ower Electronics for Green Energy Conversion*, Wiley, 2020.

[6] STMicroelectronics, "Controlling a Triac with a phototriac," ST, 2018.

[7] E. –. P. Eni, "Fault tolerant distributed control strategy for Modular Multilevel Converter in HVDC applications," Aalborg, 2013.

[8] Fairchild Semiconductor Corporation, "Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC," 2008.

[9] SEMIKRON, "Gate Resistor – Principles and Applications (AN-7003)," 2007.

[10] Semikron, "Application Note AN-7002 - Connection of Gate Drivers to IGBT and Controller," 2016.

[11] Vishay, "E Series Power MOSFET - SiHB20N50E," [Online]. Available: https://www.vishay.com/docs/91634/sihb20n50e.pdf. [Accessed 16 December 2020].

[12] "The HCPL-7520 Isolated Linear Sensing IC," [Online]. Available: https://docs.broadcom.com/doc/AV02-0956EN. [Accessed 01 April 2020].

[13] T. Clark, "Smart Power Strip," June 2011. [Online]. Available: https://drc.libraries.uc.edu/bitstream/handle/2374.UC/689377/EET2011_Clark_Tim.pdf?sequence=1. [Accessed 12 April 2021].

[14] "The TLV2474 Quad 6V, low-power rail-to-rail input/output op amp," [Online]. Available: http://www.ti.com/lit/ds/symlink/tlv2474.pdf. [Accessed 01 April 2020].

[15] R. Mancini, "Single-supply op amp design," Texas Instruments Incorporated, 2005.

[16] J. V. Farias, A. F. Cupertino, H. Pereira, S. Seleme and R. Teodorescu, "On the redundancy strategies of modular multilevel converters," *IEEE Trans. Power Del.,* vol. 33, no. 2, pp. 851-860, 2018.

[17] M. Hagiwara, R. Maeda and H. Akagi, "Negative-sequence reactivepower control by a PWM STATCOM based on a modular multilevel," *IEEE Trans. Ind. Appl.,* vol. 48, no. 2, pp. 720-729, 2012.

[18] Texas Instruments, "LM5104 High-Voltage Half-Bridge Gate Driver With Adaptive Delay," Dallas, 2014.

[19] G. J. M. d. Sousa, *Estudo de conversores modulares multinıveis (MMC) uni- e bidirecionais,* Florianopolis, 2014.