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Analysis of Double Star Modular Multilevel Topologies Applied in HVDC System for Grid Connection of Offshore Wind Power Plants

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Abstract Reducing costs related to passive elements and ensuring ability to handle short-circuit faults are essential for a reliable and cost-effective operation of modular multilevel converters (MMCs) in high-voltage direct current (HVDC) systems. HVDC systems have emerged in offshore wind power plants (OWPP), as an attractive solution to connect OWPP to the main ac system. To address these challenges, this paper carries out a benchmarking of double star (DS) MMC topologies applied to OWPP. In this sense, comparisons among DS topologies of the DSCC (double star chopper cell), DSBC (double star bridge cell) and DSHyb (double star hybrid) types are proposed. Quantitative analyses are performed, considering an OWPP of 100 MW. In the results, the topologies are compared for steady-state operation and active power dynamics. In addition, power losses and junction temperature through an one-year OWPP mission profile are analyzed. Due to dc fault tolerance and capacity to synthesize two times the converter output voltage in comparison to the DSCC, DSBC and DSHyb are best suited in HVDC systems. However, DSHyb stands out in terms of converter efficiency and capacitor energy storage. Thus, DSHyb proves to be a promising topology to connect OWPP to the ac system.

Keywords Double star topologies · Modular multilevel converter · High-voltage direct current · Offshore wind power plant.

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1 Introduction

Renewable energy sources have been massively applied in high-voltage direct current (HVDC) systems in recent decades, mainly due to the long distance in transmission lines between generation systems and customers (Jung et al, 2017). In this regard, wind power plants, especially the offshore type, allow greater energy production, compared to the onshore installation (Jung et al, 2017),(Batista et al, 2017).

The offshore installation expansion can be explained by its superior wind speed profiles compared with the onshore installation, besides the mitigation of noise, visual aspects, tower shading, among other aspects (Apostolaki-Iosifidou et al, 2019). Moreover, the offshore wind power plant (OWPP) in HVDC transmission system has been featured in facilities which are not less than 70 km away from the coast, compared with high-voltage alternating current (HVAC) (Batista et al, 2017). Regarding government policies, some countries have reduced the concessions for onshore installation.

For OWPP, voltage source converters (VSC) emerged as a topology with superior qualities compared with

line commutaded converters (LCCs) (Ghat et al, 2017). However, LCCs have been consolidated among the best converters for HVDC systems, due to their high applicability in practical projects, with good operation of transmission capacities and overcurrent (Zhao et al, 2017). On the other hand, there are disadvantages such as commutation failure and lack of black start capability. Among the VSC topologies, the modular multilevel converter (MMC) emerged as a topology with superior qualities for the HVDC system (Batista et al, 2017).

MMC must be highlighted due to its high efficiency, redundancy, low harmonic content, modularity, among other advantages (Ghat et al, 2017). This topology can be flexibly designed for several levels of output voltage (Li, 2019). Among the MMC topologies, the double star (DS) configuration is one of the most frequently applied in HVDC systems. Depending on the cell types used in the converter, different characteristics can be obtained, including: voltage levels, dc fault blocking capacity, implementation costs, among others (Sharifabadi et al, 2016; Li, 2019).

MMC application to HVDC systems has faced challenges, such as reducing costs, increasing system reliability, ability to deal with dc-link faults, and others (Xu et al, 2016). Aspects related to dc fault protection are fundamental for HVDC application (Ghat et al, 2017). Depending on the MMC cell type, this protection capability becomes inherent and makes it unnecessary to use a protection mechanism added to the converter as dc circuit breakers, which has a positive impact on the implementation costs (Wang et al, 2016).

Reference (Xu et al, 2016) presents cell types that are capable of dealing with dc fault. The most famous include, bridge cell (BC), clamp double cell (CDC), clamp single cell (CSC) and the improved hybrid (IHC) (Xu et al, 2016). The number of semiconductor devices and capacitors significantly affect the MMC costs (Dong et al, 2018), (Dong et al, 2019). Bridge cells are among the most widespread and applied in MMC-HVDC systems and present a synthesis of three voltage levels and dc fault blocking (Zhao et al, 2017).

Thus, in order to deal with the dc fault blocking capacity, make converters economically viable and handle high efficiency, the hybrid topologies are proposed in the literature (**?**), (Xu et al, 2016). In these topologies, more than one cell type is used per converter arm. By combining cells with a smaller number of semiconductors devices, as chopper cell (CC), and dc fault tolerant, as BC, the MMC is capable of dealing with the best characteristic of each one (Hofmann and Bakran, 2017), (Jung et al, 2017).

Concepts related to the hybrid topologies, such as efficiency, implementation costs, thermal characteristics of semiconductor devices and steady state operation, are still little explored when compared with traditional topologies. In this sense, this paper proposes the study of DS topologies in a OWPP of 100 MW connected to a grid of 138 kV/60 Hz, by means of two ac-dc and dc-ac stages. The converters are connected by a dc-link of 250 kV. Fig. 1 presents the schematic system diagram.

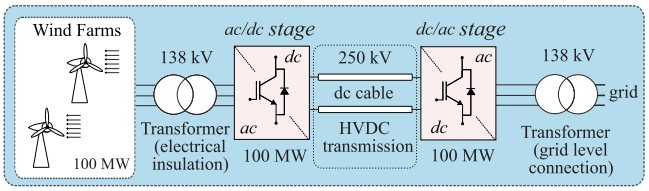

Fig. 1 Schematic system diagram - wind power plant (WPP) and transmission system: integration.

The main contributions of this paper are the following:

1. Assessment of the advantages and disadvantages of the DS MMC topologies;
2. Benchmarking of the DS topologies with respect to the steady-state performance in order to validate the design methodology adopted;
3. Benchmarking of the DS topologies with respect to the converter efficiency and thermal stresses in the semiconductor devices.

This work is organized as follows. The topology designs are detailed in Section 2. Modulation strategies for each DS topology are presented in Section 3. The control strategies are presented in Section 4. The results are discussed in Section 5. Finally, conclusions are stated in Section 6.

2 Design of Components and DS Topologies

The DS topology is characterized by the presence of multiple bi-directional cells, which are cascaded on each converter arm (Yang et al, 2018). The upper and lower arms are connected by means of two arm inductors at a common point, forming the converter phase. The arm inductor is used to limit the increasing rate of current during a fault condition on the dc-link (Sharifabadi et al, 2016).

Fig. 2 shows the DS converter structure (Cupertino et al, 2018), considering three types of cells. For the DSCC and DSBC configuration, N_C and N_B cells are arrangements per arm, respectively. The DSHyb configuration presents N_{HC} CCs and N_{HB} BCs per arm, totaling N_H cells per arm. The MMCs are powered by an HVDC transmission line, connected to the converter poles. The arm inductors are represented by L_{arm}. For one leg, the upper and lower arm voltages can be expressed as (Dong et al, 2018):

$$v_{u,n} = \frac{v_{dc}}{2} - m\frac{v_{dc}}{2}cos(\omega_1 t + \phi_n) + m\frac{v_{dc}}{12}cos(3\omega_1 t + \phi_n), \quad (1)$$

$$v_{l,n} = \frac{v_{dc}}{2} + m\frac{v_{dc}}{2}cos(\omega_1 t + \phi_n) + m\frac{v_{dc}}{12}cos(3\omega_1 t + \phi_n), \quad (2)$$

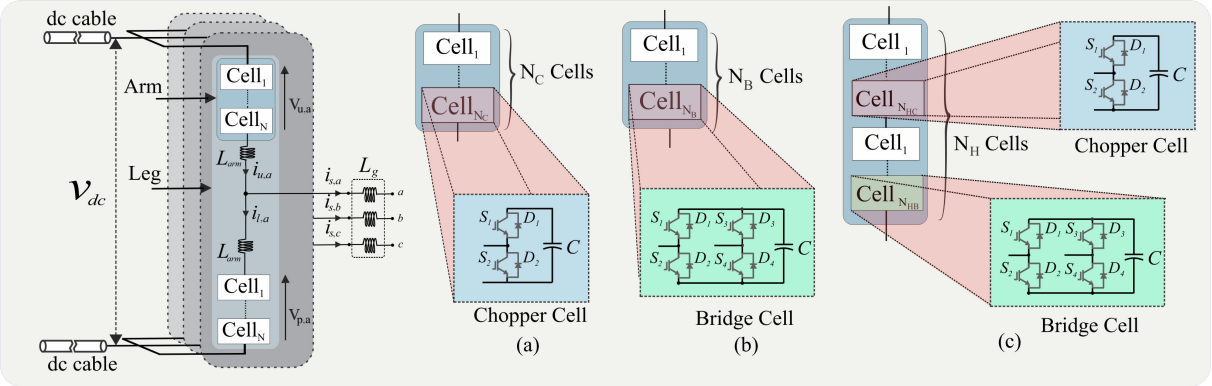

Fig. 2 Basic structure of a MMC and different cell arrangement: (a) DSCC, (b) DSBC, (c) DSHyb.

where v_{dc} is the dc-link pole to pole voltage, n is the n-th converter phase, ϕ_n is the angular displacement among the phases, m is the modulation index and ω_1 is the grid frequency.

Similarly, the upper and lower arm currents can be expressed by (Dong et al, 2018):

$$i_{u,n} = \frac{i_{dc}}{3} + \frac{i_{s,n}}{2} cos(\omega_1 t + \phi_n), \tag{3}$$

$$i_{l,n} = \frac{i_{dc}}{3} - \frac{i_{s,n}}{2} cos(\omega_1 t + \phi_n), \tag{4}$$

where $i_{s,n}(n = a,b,c)$ is the amplitude of grid current and i_{dc} is the dc-link current.

2.1 Cell Capacitance

The capacitor voltage fluctuations are directly related to the charge and discharge process of the capacitors and consequently to the power fluctuations. Therefore, the cell power expressions are derived from the product between the cell current and the cell voltage.

The energy accumulated in the cascade cells is given by the integral of the instantaneous power flowing in the arm. Thus, a maximum voltage peak fluctuation of 10% in the nominal dc capacitor voltage is obtained. (Dong et al, 2018) present expressions for the capacitor voltage fluctuations, for the CC and BC capacitance, given by:

$$C_{CC} = \frac{1.65S}{v_{dc} v_{cell} \omega_1} f_{ch}(m,\phi,t)_{pp}, \tag{5}$$

$$C_{BC} = \frac{1.45S}{v_{dc} v_{cell} \omega_1} f_{cf}(m,\phi,t)_{pp}, \tag{6}$$

where $f_{ch}(m,\phi,t)_{pp}$ and $f_{cf}(m,\phi,t)_{pp}$ are the peak-to-peak capacitor voltage fluctuations for CC and BC.

These fluctuations are directly dependent on the modulation index (m), power phase angle (ϕ) and apparent power (S). On the other hand, these fluctuations are indirectly dependent on the nominal capacitor voltage, frequency and pole-to-pole dc link. For DSCC and DSBC, the capacitance is derived from (5) and (6), respectively. For DSHyb, the BC capacitance is given by (6) which presents higher fluctuation compared to CC. CC capacitance is found, in DSHyb, in order to respect the maximum voltage peak fluctuation.

2.2 Arm Inductance

The design of the inductor is the key in the assembly converter. The inductance value is limited by the maximum current variation capacity which the semiconductor switches support. Therefore, considering a dc-link with nominal value of V_{dc} from pole-to-pole, in a limiting operation, the expression inductance is given by (Arslan et al, 2018):

$$L_{arm} = \frac{V_{dc}}{2\frac{di_{arm}}{dt}}, \tag{7}$$

where $\frac{di_{arm}}{dt}$ (kA/s) is the unit of fault current rise rate.

At first, the MMC does not have short circuit protection features. The fault current variation is expected to be limited, only by the arm inductor. Therefore, inductors with values between 0.05 and 0.15 pu are generally adopted (Harnefors et al, 2013).

3 Modulation Strategies

The semiconductor switches of CC and BC can synthesize different levels of voltage. CC has two possible states for the two gate switches, S_1 and S_2, plus a blocking state, where both are disabled. BC presents four states for the semiconductor switches with gate signal, S_1, S_2, S_3 and S_4, in addition to a blocking state, with product levels $-v_{cell}$, 0 and v_{cell}.

MMC addresses challenges associated with maintaining the capacitor voltage to form a nominal voltage level at the converter output (Ghat et al, 2017).

The nearest-level control (NLC) is a modulation method, easy to implement, and applicable to an extensive number of output voltage levels. The NLC modulation sample the cells

insertion index of the upper and lower arm ($N_{u,l}$), the arm currents ($i_{u,n}$ and $i_{l,n}$) and capacitors cell voltages ($v_{celli,j}$) at a rate f_s. The sampling rate is one of the main impact factors of the NLC modulation, since it is possible to carry out the necessary balancing of the capacitor voltages, maintaining the cell capacitor voltages between $v_{lim,l}$ ($0.9v^*_{cell}$) and $v_{lim,u}$ ($1.1v^*_{cell}$) (Sharifabadi et al, 2016).

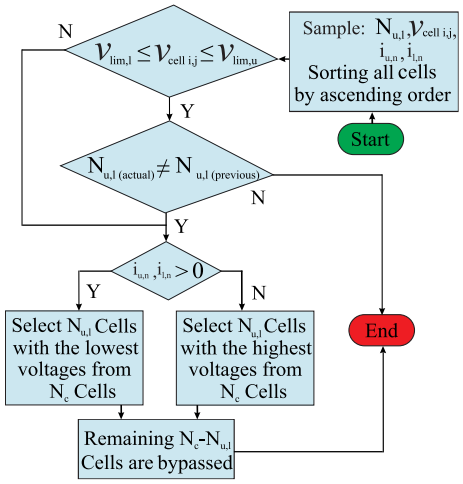

Fig. 3 Flowchart of capacitor voltage balancing of DSCC.

The NLC and sorting and selection algorithm give flexibility to the method of controlling the fluctuation of capacitor voltage. Therefore, some of the most widespread forms found in the literature are NLC algorithms with conventional sorting, cell tolerance band (CTB) and average tolerance band (ATB) (Sharifabadi et al, 2016). CTB presents a lower equivalent switching frequency, compared with PWM and ATB, which affects the semiconductor switching losses (Sharifabadi et al, 2016). Thus, the NLC-CTB are employed in this work.

Fig. 3 shows a flowchart of capacitor voltage balancing for DSCC applied in NLC modulation method. The reference voltages for cell insertions are limited between 0 and 1, which produces just positive levels in CCs. After sample the voltages of all cell capacitors, the algorithm analyzes the arm current. In case of positive arm current, $N_{u,l}$ cells with the lowest voltage in the arm are inserted, and the others ($N_C - N_{u,l}$) are remain. On the other hand, in case of negative arm current, the cells selected present the highest voltage. If all cell capacitors voltage are between $v_{lim,l}$ and $v_{lim,u}$ or the actual cells insertion index is the same of the previous cells insertion index, the NLC maintain the last insertion configuration (this condition is applied in all DS topologies).

Fig. 4 shows a flowchart of the capacitor voltage balancing for DSBC. Thus, the normalized reference voltage may be between -1/3 and 1 (He et al, 2016), (Zhao et al, 2017), where the negative reference meaning that BCs

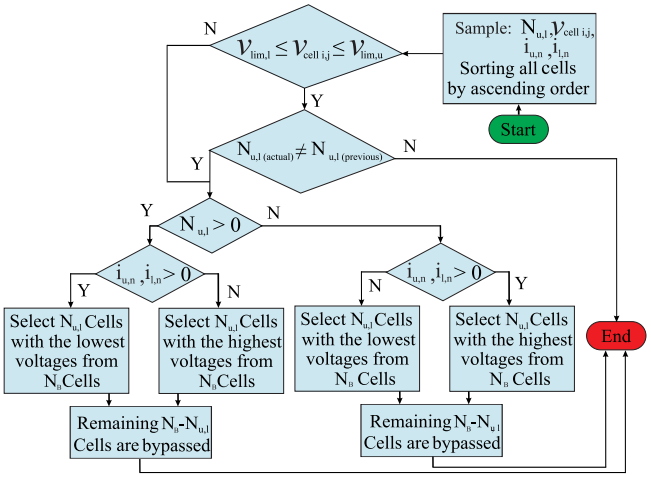

Fig. 4 Flowchart of capacitor voltage balancing of DSBC.

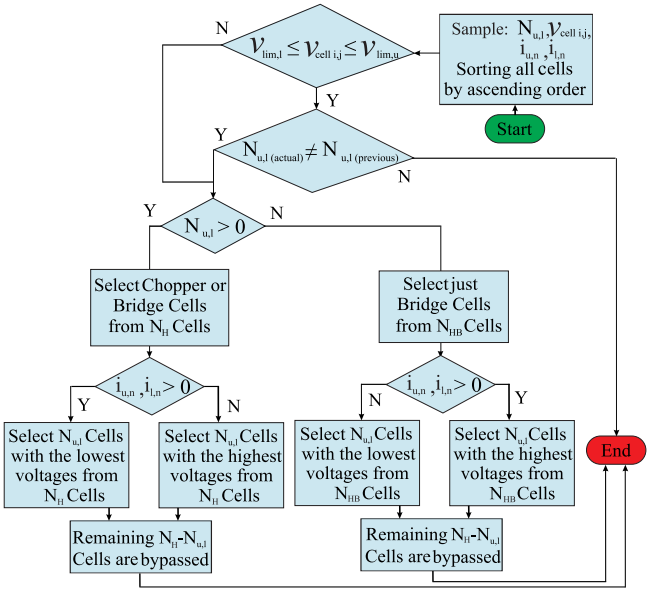

Fig. 5 Flowchart of capacitor voltage balancing of DSHyb.

synthesize a negative level (-v_{cell}). For a positive insertion index, the same analyses are performed for the insertion of the cells discussed for CCs. For a positive current value in the arm, cells with higher capacitor voltages are inserted. In case of a negative current, the cells with the smallest voltages are inserted. However, if the insertion index is below zero, the current analysis logic is the opposite, as shown in Fig. 4.

Fig. 5 shows a flowchart of capacitor voltage balancing for DSHyb. In the hybrid topology, the reference signal can be positive or negative. In the case of a negative voltage, only BCs can be inserted in the arm. On the other hand, for a positive voltage, CCs or BCs can be inserted.

4 Control Strategies

The control strategy for the DS MMC is shown in Fig. 6. The strategy performs the grid current control and the circulating current control. The individual balancing of cell voltages is executed during the CTB modulation.

The grid current control is implemented in stationary the $(\alpha\beta)$ reference frame. Thus, it is possible to carry out the simultaneous control of negative and positive sequences of the grid voltage and current.

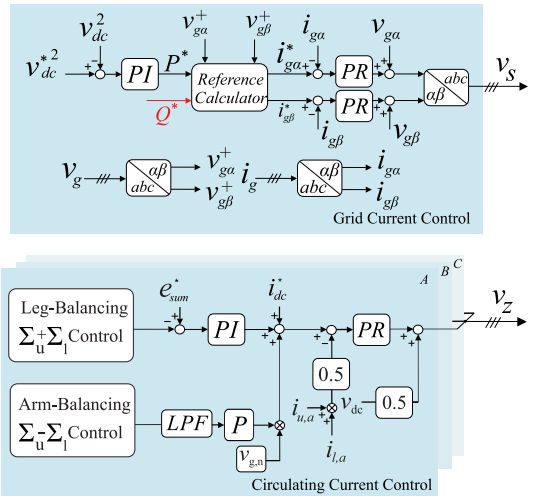

Fig. 6 Control strategies for MMC-HVDC: grid current and circulating current.

The reference calculator, presented in Fig. 6, computed the reference of active power P^* that flows from the converter to the grid. Using the instantaneous power theory (Akagi et al, 2007), it is possible to express the grid current by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{v^{+2}_{g\alpha} + v^{+2}_{g\beta}} \begin{bmatrix} v^+_{g\alpha} & v^+_{g\beta} \\ v^+_{g\beta} & -v^+_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}, \tag{8}$$

The circulating current control reduces harmonics, especially the second order harmonic, in order to promote the arm energy balancing and a MMC safe system (Li, 2019). Thus, reducing the resistive losses and inserting damping in to the converter dynamic response. The circulating current is calculated for each phase and is given by:

$$i_{z,n} = \frac{i_{u,n} + i_{l,n}}{2}. \tag{9}$$

For CTB modulation, the upper and lower reference voltages are derived from the sum of the circulating current and grid current controls, besides a component equal to half the pole-to-pole dc link, according to Fig. 6.

The normalized references to the DS topologies are expressed as follows:

$$v'_{u,n} = \frac{v_{z,n}}{v^*_{cell}} - \frac{v_s}{N v^*_{cell}} + \frac{v_{dc}}{2N v^*_{cell}}, \tag{10}$$

$$v'_{l,n} = \frac{v_{z,n}}{v^*_{cell}} + \frac{v_s}{N v^*_{cell}} + \frac{v_{dc}}{2N v^*_{cell}}, \tag{11}$$

where v^*_{cell} is the cell voltage reference and N is the total number of cells.

For the voltage reference (v_s), the injection of 1/6 pu of third harmonic is used to increase the linear operational area of the modulation curve.

The circulating current control comprises two internal loops that control the sum and the difference of the energy associated to the cell capacitors, between the upper and lower arm of each phase. Both power controls are performed with proportional and integral controllers. The external grid controls the circulating current with a resonant controller, tuned at resonant frequency modules of ω_1, $2\omega_1$ and $4\omega_1$.

The leg-balancing control employs PI controllers that produce the dc component of the circulating current in order to promote the same average voltage in each phase. The e_{sum} is computed by (Sharifabadi et al, 2016):

$$e_{sum} = \frac{C}{4}\left(\sum_{i=1}^{N} v^2_{u,i} + \sum_{i=1}^{N} v^2_{l,i}\right), \tag{12}$$

where C is the cell capacitance, $v_{u,i}$ and $v_{u,i}$ are the i-th upper and lower cell voltages, respectively.

The references for the leg-balancing control in DS topologies is given by (Dong et al, 2018).

$$e^*_{sum} = \frac{NC(v^*_{cell})^2}{2}, \tag{13}$$

The difference between the average voltage of the upper and lower arms per phase from e_{diff}, is computed for the arm-balancing control, as follows:

$$e_{diff} = \frac{C}{2}\left(\sum_{i=1}^{N} v^2_{u,i} - \sum_{i=1}^{N} v^2_{l,i}\right). \tag{14}$$

For the DSCC and DSHyb topology, the cell reference voltage is given by (15) and (16), respectively (Wang et al, 2016).

$$v^*_{cell,C} = \frac{v_{dc}}{N_C}, \tag{15}$$

$$v^*_{cell,H} = \frac{v_{dc}}{(N_H - N_{HC})}. \tag{16}$$

The $v^*_{cell,H}$ considers the maximum number of BCs in DSHyb that produce negative state. For the case study, the N_{HB} satisfies the relation to dc-link fault protection and performs the maximum output voltage. The maximum relation between N_{HB} and N_H that returns a higher output

voltage is 1/3, in order to allow sufficient charging and discharging times for the CCs to balance their voltages within each fundamental period (Zeng et al, 2015). Similarly, the cell reference voltage for the DSBC considers the maximum output voltage, as given by (Jocvic et al, 2017):

$$v^*_{cell,B} = \frac{1.5 v_{dc}}{N_B}. \tag{17}$$

In order to ride through to dc short-circuit fault, BCs need to compensate the maximum negative voltage output per arm (Dong et al, 2018). Therefore, the N^*_B requirement for the DSBC and DSHyb is given by:

$$N^*_B = \frac{max(v_{u,n})}{v^*_{cell}}. \tag{18}$$

5 Power Losses: Thermal Model and Inductor Losses

Parameters of power losses and operating temperatures of the semiconductors affect the lifetime and reliability of the converter. In the analyses of thermal circuits, the junction, case and heat sink temperatures are the main variables that affect power losses (Zeng et al, 2015).

The thermal circuit under study is formed by the Cauer and Foster models, as observed in Fig. 7. The multi-layer Foster model estimates the junction temperature of the semiconductors. The power losses of the semiconductors are estimated by the Cauer equivalent model and multi-layer Foster model. The data from the multi-layer Foster model and equivalent Cauer model are extracted from the datasheets of the used semiconductor switches.

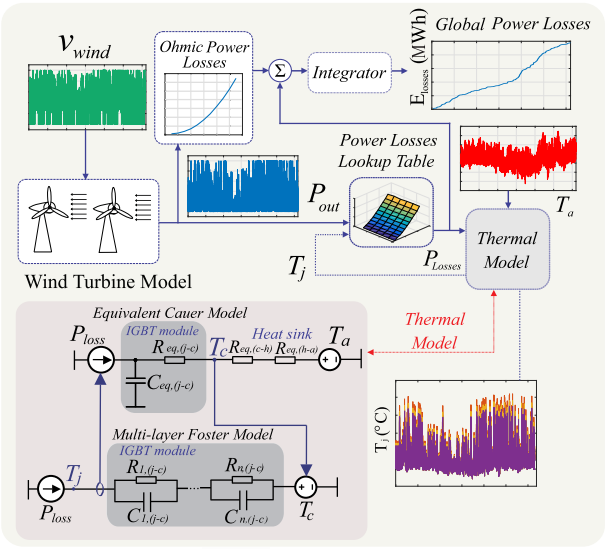

Fig. 7 Computing scheme of global power losses.

Heat sinks are designed per cell to ensure that the steady-state junction temperature T_j of the semiconductor device is within a safety limit. For the case study, the maximum junction temperature is 110° C. It is applied only the thermal resistance of the heatsink, since its capacitive effect is much greater than those presented by the semiconductor models.

The IGBT module from Infineon FZ400R65KE3 (400 A/6500 V/150° C) is chosen as power semiconductor device. In order to obtain the power losses, the conduction and switching losses are achieved from lookup tables. The lookup tables are derived from the datasheet power loss curves.

The power losses in the arm inductor are approximated by the ohmic losses associated with intrinsic resistance (R_{arm}). Thus, the total energy dissipated was calculated from (19).

$$e_{Larm} = 6R_{arm} \int i^2_{u,a} dt \tag{19}$$

6 Case Studies

In order to compare the three DS topologies, it is considered a case study of an offshore MMC wind power transmission system with nominal power of 100 MW and a transmission voltage of 250 kV. The dc-link base is considered in pu calculation. The main parameters of the DS topologies are shown in Table 1. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method. Simulations are performed in PLECS and Matlab/Simulink environment to benchmarking the DS topologies.

The first case study considers the following conditions of MMC-HVDC operation:

- $0 \leq t \leq 0.5$ s: OWPP injects 0.5 pu of active power into the power grid;
- $0.5 \leq t \leq 0.52$ s: OWPP increases from 0.5 to 1 pu with a ramp of 10,000 MW/s;
- $0.52 \leq t \leq 1$ s: OWPP injects 1 pu of active power into the power grid;

The implemented CTB modulation maintaining the cell capacitor voltages between $v_{lim,l}$ of $0.9v^*_{cell}$ and $v_{lim,u}$ of $1.1v^*_{cell}$, for all DS topologies.

The controller parameters are shown in Table 2. The computation of the control parameters follow the methodology discussed in the references (Sharifabadi et al, 2016), (Yepes et al, 2011). The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method.

In the second case study, a theoretical one-year mission profile was used to analyze the junction temperature and power losses of semiconductor devices. The wind speed

Table 1 Parameters of the MMC-HVDC systems.

	DSCC	DSBC	DSHyb
Active power	100 MW	100 MW	100 MW
Rated dc voltage	250 kV	250 kV	250 kV
Rated dc current	400 A	400 A	400 A
Rated ac voltage	138 kV	276 kV	276 kV
Arm nominal voltage	250 kV	375 kV	341.25 kV
Arm inductance (0.05 pu)	16.8 mH	67.2 mH	67.2 mH
Arm resistance (X/R = 18)	0.35Ω	1.4Ω	1.4Ω
Cell capacitance	1 mF	1.2 mF	1.2/0.2 mF
Cell reference voltage	3.25 kV	3.25 kV	3.25 kV
Cells number	77	115	70BC/35CC

Table 2 Parameters of the controllers.

Gain	DSCC	DSBC	DSHyb
Prop. of dc-link control ($\times 10^{-4}\Omega^{-1}$)	9.95	9.95	9.95
Integral dc-link control (Ω^{-1}/s)	0.0256	0.0256	0.0256
Prop. of grid current control (Ω)	499.53	1498.6	1709.6
Resonant of grid current control (Ω/s)	1000	1500	1000
Prop. of leg-balancing control ($\times 10^{-8}V^{-1}/s$)	2	2.25	10
Integral of arm-balancing control ($\times 10^{-8}V^{-1}$)	10	10000	1
Prop. of circulating current control (Ω)	3.4	1.5	2.5
Resonant of circulating current control (Ω/s)	300	150	150
Prop. of arm-balancing control ($\times 10^{-7}V^{-2}/s$)	2	8.89	2

mission profile is based on measurements in Southern Brazilian. The data were measured at 20 meters with a sampling time of 15 minutes and translated to 100 meters using the logarithmic law (Tizgui et al, 2017), as presented in (20).

$$v_w(h) = v_{ref}\left(\frac{h}{h_{ref}}\right)^{\alpha}, \tag{20}$$

where v_{ref} is the reference wind speed, h_{ref} is the reference height and α is the boundary layer exponent.

The pitch limits for speed in generator is cut in the rated speed of 14.5 m/s (upper limit) and 3 m/s (lower limit). Thus, the OWPP nominal power was set to 100 MW and the wind turbine power is derived by (21) (Ouyang et al, 2019).

$$P_{WT} = \frac{\rho}{2}A_{WP}c_p(\lambda,\theta)v_w^3, \tag{21}$$

where ρ is the air density, A_{WP} is the blade rotation area, c_p is the power coefficient, λ is the tip speed ratio and θ is the pitch angle. Fig. 8 shows the one-year OWPP profile of ambient temperature, wind speed and generated power.

7 Simulation Results

Fig. 9 shows the performance for the grid current in the first case study, for the three DS topologies. All topologies presented a 20 ms transient response. The observed total harmonic distortion (THD) for the nominal power operation revealed higher distortion for DSHyb (0.57%). In turn, DSCC and DSBC showed distortions of 0.53% and 0.50%, respectively. The differences in terms of harmonic content revealed a negligible difference among the topologies.

The circulating current for phase a is shown in Fig. 10. It is observed that the circulating current has a dc characteristic component, necessary for active power exchange between

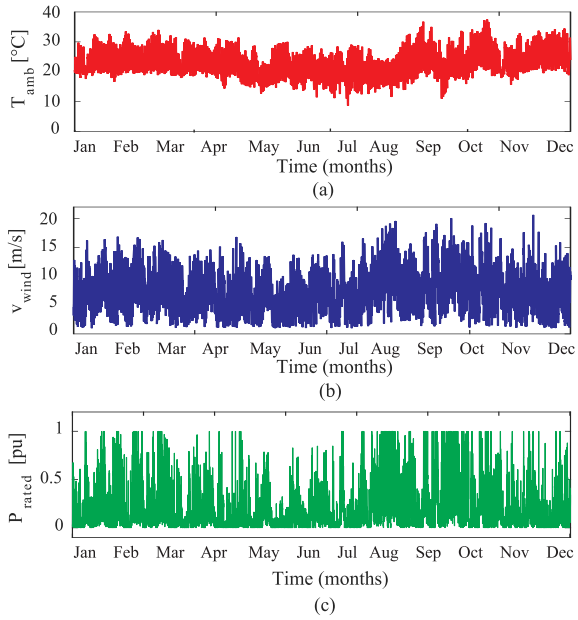

Fig. 8 One-year mission profile from an offshore wind farm. (a) ambient temperature, (b) wind speed, (c) generated power.

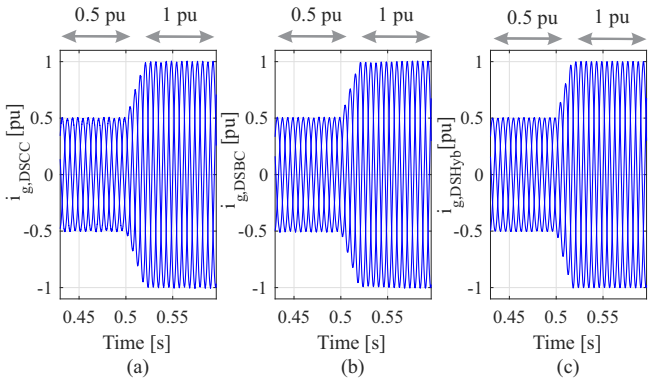

Fig. 9 Grid current i_g for: (a) DSCC, (b) DSBC, (c) DSHyb.

the dc-link and the grid. It is possible to verify that the circulating current dc component increases proportionally to the injected power. The circulating current in the DSHyb topology, shown in Fig. 10 (c), has a fluctuation of 0.123 pu. This topology presents the highest level of peak-to-peak fluctuation in the circulating current. The other topologies, DSCC (Fig. 10 (a)) and DSBC (Fig. 10 (b)), presented fluctuations of 0.107 pu and 0.065 pu, respectively.

The results for the upper arm capacitor voltages in phase a of the DSCC, DSBC and DSHyb topologies are presented in Fig. 11. The cell capacitor voltages are present in injection of 0.5 pu and 1 pu of rated active power. All capacitances present in DS topologies are designed in order to respect the tolerance level of cell voltage (± 10% of v^*_{cell}). Fig. 11 (a) presents the DSCC cell capacitor voltages and Fig. 11 (b) details the shape of cell capacitor voltages in rated operation. The greater spread of the waveforms for the CCs is explained by the fact that any cell can enter during the

Table 3 Comparison of operation for different types of DS topology.

	DSCC	DSBC	DSHyb
Grid characteristics	138 kV/ 0.59 kA	276 kV/ 0.295 kA	276 kV/ 0.295 kA
Output level numbers	78	116	106
Numbers of IGBTs per arm	(2x77) = 154	(4x115) = 460	(4x70 + 2x35) = 350
THD of grid current	0.53 %	0.50 %	0.65 %
Fault blocking capability	no	yes	yes
Semiconductor power losses (one-year - mission profile)	328.86 MWh	1,174.81 MWh	822.76 MWh
Inductor losses (one-year - mission profile)	78.31 MWh	151.78 MWh	151.78 MWh
Total converter losses (one-year - mission profile)	407.17 MWh	1,326.59 MWh	974.54 MWh
Converter efficiency (1 pu of power injected)	99.51 %	98.36 %	98.81 %
Capacitor energy storage (kJ/MW)	24.39	43.73	26.62
Inductor energy storage (kJ/MW)	9.76	12.46	12.46
Heatsink resistance (K/kW)	85	35	105/19.5
Equivalent switching frequency (1 pu of power injected)	205 Hz	181 Hz	227 Hz

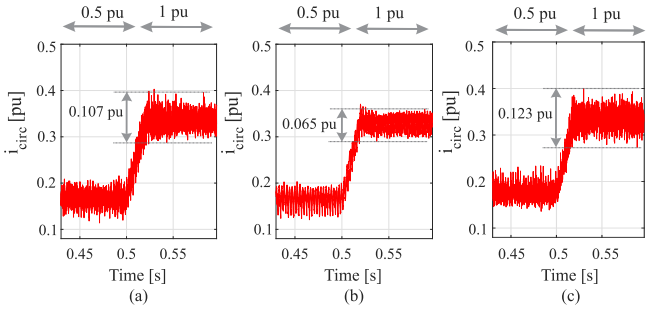

Fig. 10 Circulating current (i_{circ}) for (a) DSCC (b) DSBC (c) DSHyb.

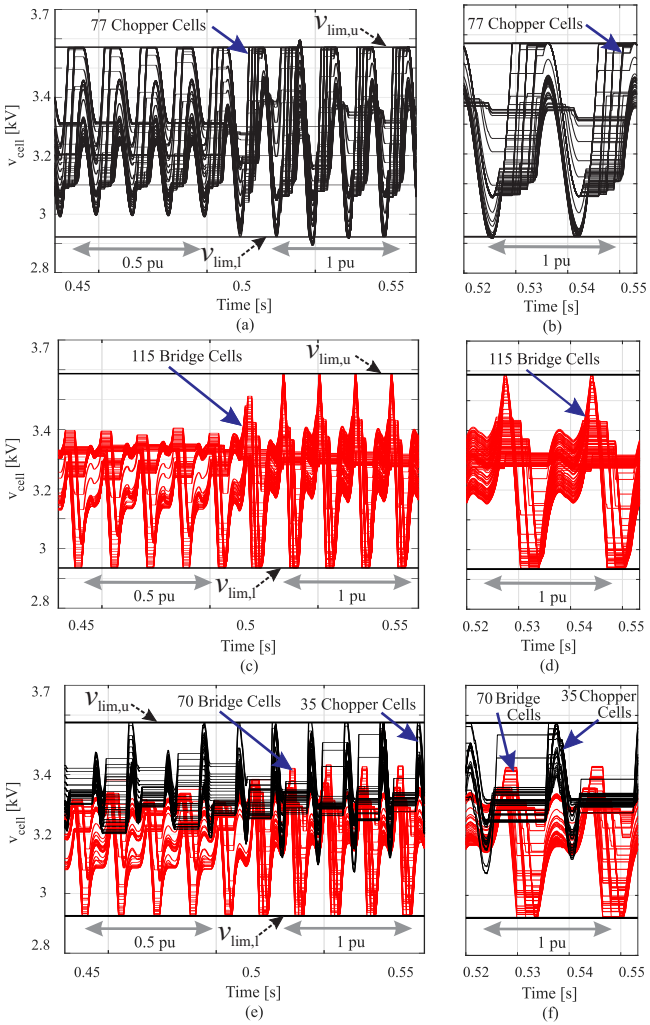

Fig. 11 Upper cell capacitor voltages for (a) DSCC, (b) detailed cell voltage, (c) DSBC, (d) detailed cell voltage, (e) DSHyb, (f) detailed cell voltage.

operation of the converter. The reference voltage applied to the modulation is always positive (limited between 0 and 1). This topology requires a capacitance of 1 mF for the tolerance level established.

Fig. 11 (c) presents the DSBC cell capacitor voltages and Fig. 11 (d) details the shape of cell capacitor voltages in rated operation. For this topology, the BCs are able to produce negative levels (reference voltage is limited between $-\frac{1}{3}$ and 1). Under such conditions, the other cells are bypassed, which produces a higher level of horizontal lines in the negative insertion index. This topology requires a capacitance of 1.2 mF for the tolerance level established.

Fig. 11 (e) presents the DSHyb cell capacitor voltages and Fig. 11 (f) details the shape of cell capacitor voltages in rated operation. CC capacitor voltages distribution reaches just upper tolerance limit, because the CCs are inserted only in positive insertion index. It is require the capacitance of 0.2 mF for CC in the upper tolerance level established. On the other hand, the BCs distribution reaches the lower tolerance limit and requires 1.2 mF (six times greater than the CCs in the DSHyb) for the lower tolerance level established. Therefore, the BCs, in DSHyb, present a higher capacitance due to the operation in positive or negative insertion index.

Tab. 3 presents a comparison among the DS topologies, considering different parameters. The DSBC topology presented a high number of IGBTs per arm, using approximately 31% more semiconductor devices than DSHyb. As both have protection capacity against dc-link faults, DSHyb presents a better cost-benefit ratio in terms of semiconductor devices, as evidenced by the number of IGBTs per arm.

The volume associated with the passive elements, presented in Tab. 3, such as the arm inductor and the capacitors, can be quantified in terms of the maximum energy accumulated. This analysis is fundamental to quantify the converter costs. The volume of the inductors for the DSBC and DSHyb topologies presented an occupancy 28% superior to DSCC. Besides, the volume occupied by the capacitors was also greater for the DSBC and DSHyb topologies.

The global power losses are computed in terms of the semiconductor power losses and arm inductor losses. In this regard, it is possible to quantify the efficiency of the converter by means of different levels of active power injection. With an increment of 0.1 pu, it is analyzed the efficiency of the topologies between 0.1 pu and 1 pu. DSCC presented, for any power injection condition, efficiency higher than 99.5%, as shown in Fig. 12. DSBC and DSHyb topologies presented efficiencies higher than 98.3% (for 1 pu), with a considerable advantage of DSHyb.

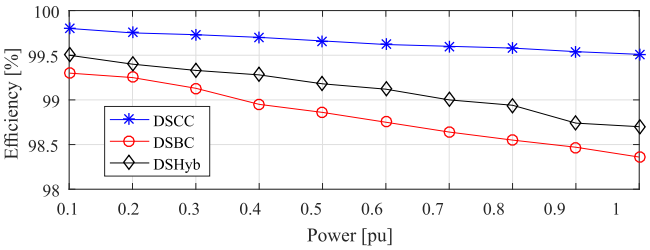

Fig. 12 Efficiency for each converter topology at various active power levels.

The one-year mission profile is applied, for the analysis of the performance of the junction temperature of the semiconductor switches with the highest T_j peak. Fig. 13 (a), (c) and (e) present the dynamics of T_j during the one-year mission profile for the DSCC, DSBC and DSHyb topologies, respectively. Fig. 13 (f) shows that the temperature for the IGBT S_2(CC) in DSHyb is less stressed than for IGBT S_1(BC) and IGBTs in DSCC and DSBC, once several junction temperatures are close to 80° C. DSCC and DSBC required a heat sink resistance of 35 and 85 K/kW, respectively. DSHyb presented a value of 105 K/kW for CC and 19.5 K/kW for BC.

The global power losses are based on conduction and switching losses of the IGBTs and diodes and arm inductor losses. In this regard, the DSCC topology presented less than half of the total losses in relation to the others topologies. This relation can be explained by the smaller use of cells and semiconductors in DSCC, which has three times less IGBTs per arm than DSBC. On the other hand, the equivalent switching frequency presented a value of 227 Hz for DSHyb, which reveals a higher level of switching for this topology when it is considered a same dc-link with the same nominal power.

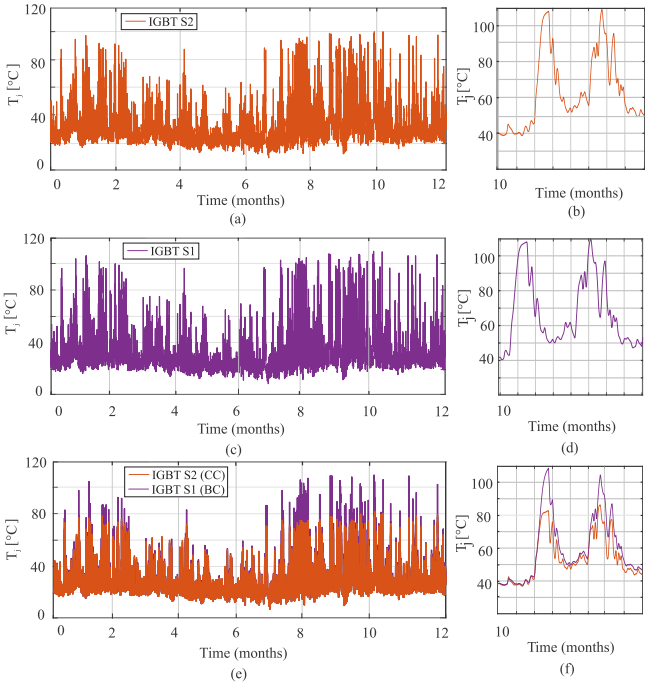

Fig. 13 Junction temperature for the most stressed semiconductor device on one-year mission profile for (a) DSCC, (b) maximum T_j detailed for DSCC, (c) DSBC, (d) maximum T_j detailed for DSBC, (e) DSHyb, (f) maximum T_j detailed for DSHyb.

8 Conclusions

This paper presented a benchmarking among three DS MMC topologies applied to HVDC systems with OWPP. The results are divided into two case studies. The first one compared the topologies in terms of steady-state operation and active power dynamics. The second case study analyzed the power losses and junction temperature through an one-year OWPP mission profile.

The steady-state results revealed a similar response for the terminal characteristics, such as grid current, with THD levels close to 0.5% for all topologies. For DSHyb, BCs exhibit six times the CC capacitance. DSCC allows the operation of lower capacitance, in relation to DSBC. Thus, DSBC requires more investments in capacitor energy storage. In terms of the mission profile analysis, the global power losses of DSCC decreased by 70% and 58% in relation to DSBC and DSHyb, respectively. Nevertheless, DSBC and DSHyb present dc fault tolerance and synthesize two times the converter output voltage in comparison to DSCC.

Therefore, DSHyb and DSBC are more suitable in HVDC systems. However, DSHyb stands out in terms of converter efficiency and capacitor energy storage, which

significantly affects operational and implementation costs. Thus, DSHyb proves to be a promising topology to connect OWPP to the ac system.

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