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On the Redundancy Strategies of Modular Multilevel Converters

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***Abstract*—The modular multilevel converters (MMCs) have become an attractive topology in recent years. The MMC has been employed in several applications as HVDC, energy storage, renewable energy, electrical drives and STATCOMs. One of advantages of MMC based topologies is the inherited fault-tolerant operation associated with the high number of submodules (SMs). This work proposes the study of four redundancy strategies which can be employed in modular multilevel converters: Standard Redundancy (SR); Redundancy Strategy based on Additional Submodules (RAS); Redundancy Strategy based on Additional Submodules Optimized (RASO); and Redundancy Strategy based on Spare Submodules (RSS). These strategies are compared through a case study of a 15 MVA MMC STATCOM. A new approach for the SM capacitance design is proposed, including the effect of the negative sequence current in the converter storage energy variations. The comparisons of the redundancy strategies are accomplished based on dynamic behavior, capacitor voltage balancing, control complexity and power losses. Finally, the advantages and drawbacks of each redundancy strategy are presented.**

***Index Terms*—Modular Multilevel Converter; Redundancy strategies; Positive and negative sequence injection; Power losses.**

I. Introduction

In recent years, the modular multilevel converter (MMC) has become the most attractive multilevel converter topology [1]. The concept of MMC consists in obtaining a high voltage converter for high power applications by means of a cascade connection of converters with smaller voltage (known as submodules - SMs). As advantages of MMC converter topologies, it can be highlighted [1], [2]:

- Low switching frequency, resulting in a converter with high efficiency;
- A higher number of levels can be reached;
- Design flexibility, since the rated voltage can be increased by including more SMs;
- High reliability.

The MMC has been employed in several applications as HVDC, energy storage, renewable energy, electrical drives and STATCOMs [1]. Many works in literature have proposed modulation techniques, capacitor balancing techniques and circulating current strategies for MMCs [1], [2]. Nevertheless, the operation of the converter when faults occur in one or more SMs is an important issue seldom reported in literature.

The MMC topology is often featured with its robustness in terms of SM failures. When power switch failures are identified (generally by advanced gate drives), the corresponding SM should be bypassed [3]. In order to ensure that the converter remains operational at this condition, some redundancy strategy needs to be included to the converter structure [4]. Therefore, the operation of the converter can continue without affecting the overall performance [5]. This condition is attended for a perceptual number of SM failures. In most works in literature, the redundancy factor is something around 10 % [6]. This means that the converter operation can continue if less than 10 % of the SMs fail.

Reference [7] classify the MMC redundancy strategies into two schemes: hot reserve and cold reserve. In hot reserve based strategies the redundant SMs operate in the same way as other SMs. When a fault occurs, the faulty SM is bypassed while the MMC keeps working correctly [7], [8]. In cold reserve based strategies the redundant SMs are bypassed and discharged. When a fault occurs, the corresponding faulty SM is bypassed and the redundant SM is inserted into the main circuit [7], [8]. Thereby, the hot reserve based strategies can lead to asymmetrical operation in the converter and larger power losses, while the cold reserve based strategies presents more significant transients during failures.

Nevertheless, it is possible to explore the redundancy of the MMC without use additional SMs. Therefore, the terminology proposed by [7] is to some degree incomplete. Alternatively, this work classifies the redundancy strategies employed in modular multilevel converters into 4 strategies: Standard Redundancy operation (SR), Redundant operation based on Additional SMs (RAS), Redundant operation based on Additional SMs Optimized (RASO) and Redundant operation based on Spare SMs (RSS).

References [5], [6], [9] and [10] propose the MMC operation with the standard redundancy operation. In SR, when a SM fails, the voltage in the operating SMs is increased. The number of levels at the converter output is reduced

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while the overmodulation is avoided [5], [6]. According to [5], since MMC has been built with hundreds of SMs per phase leg, degrading the output voltage level would be an economic solution. Nevertheless, in practical applications, the safe operating area of the SMs is generally 50 - 60 % of the semiconductors rated voltages. Therefore, the SR redundancy factor is limited by the maximum voltage stresses at the semiconductor devices and capacitors.

The RAS strategy consists in operating the converter with more SMs than the rated number. When a SM fails, it will be bypassed and the control strategy will be dynamically adapted for the new number of SMs [11], [12]. Two approaches are possible: In the first approach, all SMs are controlled at the rated voltage. Therefore, when a SM fails, the voltage of operating SMs does not need to be increased. Therefore, less significant transients are observed in capacitor voltages. However, RAS results in more switching losses in steady-state and this fact can affect the converter efficiency [6]. A second approach consists in operating the SMs with reduced voltage under normal conditions. In this case, the voltage stresses in the SM power devices are reduced. Therefore, the switching losses are reduced, leading to an increase in the converter efficiency. Therefore, this strategy is referred in this paper as optimized redundant operation based on additional SMs (RASO). In the RASO strategy when some failure happens, the voltage at the SMs is increased in order to avoid overmodulation.

Finally, the RSS is based on the spare SMs concept [3]. Under normal conditions, the spare SM is always bypassed [7]. When a SM fails, it is replaced by a spare SM. The spare SM is then charged by the control strategy. It can be noted that RSS does not change the number of operating SM of the MMC. Therefore, any control adaptation is employed. However, if compared to the other strategies, RSS results in a larger transient unbalance in capacitor voltages, since the spare SM is discharged when it is inserted into the MMC circuit. In fact, each power module has bleeder resistors installed in parallel with the SM capacitor to provide a discharge path for the capacitor when the converter is shutdown [13], [14]. Furthermore, some manufacturers generally use these resistors to make voltage divider for achieving a low-voltage input to an auxiliary power supply, which is further employed to power up the SM control card [15]. Therefore, when spare SM is inserted, it cannot immediately operate requiring a period of time to charge its capacitor to nominal voltage value [7], [8].

Reference [7] discusses the application of the RSS strategy in a MMC-HVDC system. A new control method for MMC is proposed to seamlessly ride through the period when bypassing a faulty SM and inserting a redundant SM. The RAS strategy is approached by [8] considering asymmetrical operation of the converter arms. A mathematical model of the MMC with arms containing different numbers of SMs is developed. However, the effect of the redundancy in the MMC efficiency was not approached.

Reference [3] combines RAS and RSS to extend the MMC redundancy factor, which is modulated by the nearest level control (NLC) strategy. Whereas failures happen, the RAS strategy is employed. If the number of failures exceeds the number of additional SMs, RSS is employed to avoid an extreme emergency or catastrophic failure. Nevertheless, no comparison about power losses was presented by this reference.

On the other hand, reference [6] compares the dynamic behavior of two redundancy strategies applied in MMC: the first approach employs both SR and RAS with direct modulation. In the second approach, the average voltage of the SMs is maintained constant even during failures, as discussed in [16]. Again, no analysis in terms of power losses was presented. Additionally, few works in literature analyze the redundant operation when phase-shift modulation is employed.

Thereby, a detailed comparison and analysis of redundancy strategies applied in MMC has been missing in literature. This paper aims to fill this void. The four redundancy strategies previously described are compared considering a 15 MVA MMC. The STATCOM application is taken into account. This application presents important control tasks, once unbalanced currents can flow through the converter during injection of both positive and negative sequence reactive power into the power system.

In view of the points aforementioned, this work provides the following contributions:

- Design of MMC based STATCOM, considering the 4 redundancy strategies for both positive and negative sequence injection;
- Discussion of the necessary changes in the control strategy when additional SMs are employed, considering phase-shift modulation;
- Comparison of the dynamic performance of the redundancy strategies when both positive and negative sequences are compensated by a MMC STATCOM;
- Evaluation of the converter power losses when redundancy strategies are employed.

The study is outlined as follows. Section II presents the MMC STATCOM topology and the control strategy. The necessary modifications in the control strategy for each redundancy strategy is discussed. The design of the MMC considering the redundancy strategies and negative sequence compensation is presented in Section III. Section IV presents the case study and the parameters of the simulated model. The obtained results are discussed in Section V. Finally, the conclusions of this work are stated in Section VI.

II. Modular Multilevel Converter

The topology of the MMC STATCOM studied in this work is illustrated in Fig. 1. As observed, a double-star chopper cell (DSCC) topology is chosen. Each cell contains a SM capacitance C and two semiconductor switches. The arm inductance L_{arm} is responsible for reducing the high order harmonics in the circulating current and also limiting the currents during faults [17]. Typically, the per unit (pu) arm inductance values for grid connected converters are in the range of 30 % [18]. The converter is connected to the main grid through a three-phase transformer with inductance L_g. Generally, in parallel with each SM, there is a switch S_T, which is responsible to bypass it in case of failures [19]. This

switch can also be used to maintain the spare SMs bypassed while the MMC is operating normally [3]. N operating SMs and M additional SMs are considered per MMC arm. R_b represents the bleeder resistor.

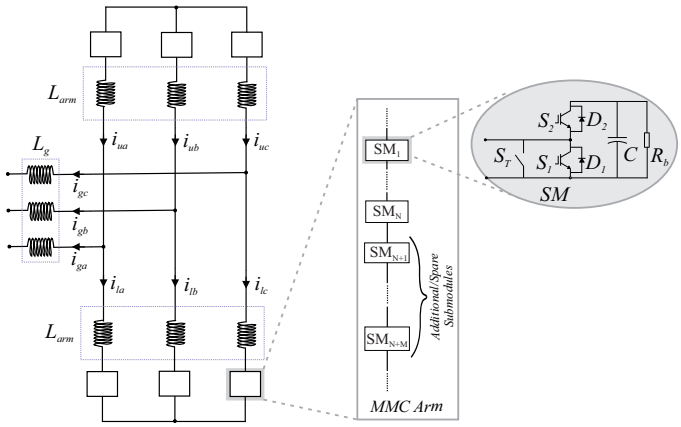

Fig. 1. Schematic of the DSCC-MMC STATCOM.

The proposed control strategy for the MMC STATCOM is presented in Fig. 2. The grid current control is responsible for injecting the positive and negative sequence reactive power into the grid. This strategy is performed by the inner loops implemented in stationary ($\alpha\beta$) reference frame, which results in a simultaneous control of positive and negative sequence currents. Basically, the external loop controls the square of the average voltage v_{avg} of all SMs of the converter. This average voltage is computed by:

$$v_{avg} = \frac{1}{N_T}\sum_{i=1}^{N_T} v_{sm,i}, \tag{1}$$

where $v_{sm,i}$ is the ith SM voltage. N_T is the total number of operating SMs, given by:

$$N_T = \sum_{j=1}^{6} N_{o,j}, \tag{2}$$

where $N_{o,j}$ is the number of operating SMs of the arm j.

The average voltage reference v^*_{avg} is dependent on the redundancy strategy employed. For RAS and RSS strategies, the voltage of all SMs is controlled according to the reference value $v^*_{sm,j}$, given by:

$$v^*_{sm,j} = \frac{v_{dc}}{N}, \tag{3}$$

where v_{dc} is the nominal MMC effective dc-link voltage. Although no physical dc-link is present in double star MMC STATCOM, this value is an important parameter to avoid overmodulation [20]. Even during failures, the reference voltages of the SMs for RAS and RSS strategies do not change. In this case, the average voltage is given by:

$$v^*_{avg} = \frac{v_{dc}}{N}. \tag{4}$$

On the other hand, when RASO and SR strategies are employed, the SMs voltage reference at the failed arms is

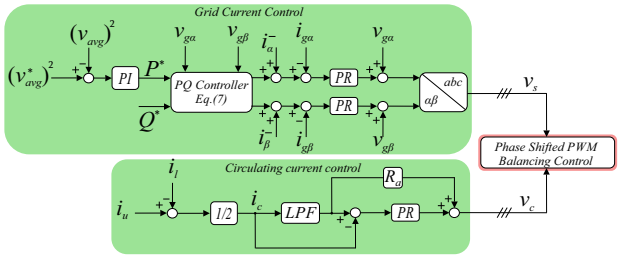

Fig. 2. Proposed control strategy for MMC-STATCOM.

increased. In this case, the voltage reference is computed separately per arm. Accordingly,

$$v^*_{sm,j} = \frac{v_{dc}}{N_{o,j}}. \tag{5}$$

Therefore, the average voltage references v^*_{avg} for RASO and SR strategies are calculated by:

$$v^*_{avg} = \frac{6}{N_T} v_{dc}. \tag{6}$$

The average voltage loop calculates the necessary active power P^*, that flows to the converter. Using the instantaneous power theory [21], it is possible to obtain expressions for the grid current reference by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{v^2_{g\alpha} + v^2_{g\alpha}} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}, \tag{7}$$

where $v_{g\alpha}$ and $v_{g\beta}$ are the stationary components of the grid voltage. Proportional resonant (PR) controllers are employed in order to track the reference current. The dynamics of the grid current in the stationary reference frame is given by [22]:

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} + L_{eq}\frac{di_{g,\alpha\beta}}{dt} + R_{eq} i_{g,\alpha\beta}, \tag{8}$$

where $L_{eq} = L_g + 0.5L_{arm}$, $R_{eq} = R_g + 0.5R_{arm}$ and $v_{s,\alpha\beta}$ is the equivalent output voltage of the MMC. Using this dynamic model, the PR controllers can be adjusted using the design methodology proposed by [23]. Feedforward actions of the grid voltage are included in order to improve the dynamic behavior.

The circulating current control is responsible for reducing the harmonics in the circulating current and inserting damping in the converter dynamic response. The circulating current is calculated per converter leg and is given by [2]:

$$i_c = \frac{i_u + i_l}{2}. \tag{9}$$

The dynamics per phase of the circulating current is given by [17]:

$$v_c = L_{arm}\frac{di_c}{dt} + R_{arm} i_c, \tag{10}$$

where v_c is the STATCOM internal voltage. As stated in [17], the circulating current dynamics is stable. However, the damping obtained is related with the arm resistance R_{arm}, whose value is very small. Therefore, a circulating current

loop based on a proportional controller is inserted into the control strategy in order to increase the damping [17], [24].

Fig. 2 presents the circulating current control loop. Since convergence is guaranteed even without circulating current control, the circulating current reference i_c^* is obtained through low-pass filtering of i_c [17]. A butterworth second order filter is employed.

Regarding negative sequence injection, a considerable 2nd harmonic component appears in the circulating current [25]. This second order component generally cannot be compensated by the proportional controller [26]. In view of this problem, a resonant controller tuned to the 2nd harmonic is added to the circulating current control.

The reference voltages v_s and v_c are inputs of the modulation strategy. This paper uses the phase shift pulse width modulation (PS-PWM) method [2]. In this technique, each SM has its own carrier wave, which is phase shifted from the other SM carriers. The switching signals are generated by the comparison of the normalized reference signals $v_{u,n}$ and $v_{l,n}$. The corresponding SM is inserted into the arm when the reference amplitude is above the carrier. When the reference amplitude is below the carrier, the corresponding SM is bypassed. The switching frequency of the SMs is defined by the carrier frequency [27].

In the PS-PWM method, an extra individual balancing control loop is necessary to maintain the capacitor voltages following the reference $v_{sm,j}^*$. As suggested in [2], a proportional controller k_b is employed. In this case, the individual balancing control law is given by:

$$v_b = k_b(v_{sm,j}^* - v_{smf,i})sign(i_{sm,i}), \tag{11}$$

where $i_{sm,i}$ is the current which flows by the SMs. For upper arms, $i_{sm,i} = i_u$ and for lower arms, $i_{sm,i} = i_l$. $v_{smf,i}$ is obtained from the individual capacitor voltages through a moving average filter. This filter is responsible for attenuating the capacitor voltage ripple and improving the individual balancing performance [28]. In such conditions, the normalized reference signals per phase are given by:

$$v_{u,n} = v_b + \frac{v_c}{v_{sm,u}^*} - \frac{v_s}{v_{sm,u}^* N_{o,u}} + \frac{1}{2}, \tag{12}$$

$$v_{l,n} = v_b + \frac{v_c}{v_{sm,l}^*} + \frac{v_s}{v_{sm,l}^* N_{o,l}} + \frac{1}{2}. \tag{13}$$

where $N_{o,u}$ and $N_{o,l}$ are the number of operating SMs in the upper and lower arms, respectively.

Finally, for RAS, RASO and SR strategies, the number of operating SMs and the number carrier change accordingly. Thus, the phase displacement of the carriers needs to be adaptive. Therefore, the angle displacement of the carriers is calculated by the following equation:

$$\theta_{c,n} = 2\pi \left(\frac{n-1}{N_{o,j}} \right). \tag{14}$$

where $n = 1, 2, ..., N_{o,j}$. As observed, the carriers are generated independently for each arm.

The relations (12)-(14) are general and they can be employed for any MMC application, as well the redundancy strategies previously discussed. Nevertheless, according to the application, different control approaches may be implemented to determine the variables v_b, v_c and v_s.

III. Design of MMC STATCOM with redundancy

A. Number of SMs

In the case study proposed in this work, a STATCOM of 15 MVA and a line voltage of 13.8 kV at the point of common coupling (PCC) is considered. The first step in the MMC design is the definition of the effective dc-link voltage v_{dc}. The following considerations are assumed:

- The variation in grid voltage is 5 %;
- The STATCOM output impedance in pu is considered 18 % with a variation of 5 % around this value;
- The effective dc-link voltage presents in the worst case 10 % of ripple and a constant error of 3 % in steady-state.

Under these conditions, the line voltage synthesized by the STATCOM V_s is given by [20]:

$$V_s \approx 1.25 V_g, \tag{15}$$

where V_g is the PCC line voltage.

Considering the sinusoidal modulation, the effective dc-link voltage is given by [20]:

$$v_{dc} = \frac{2\sqrt{2}}{0.87\sqrt{3}} \frac{V_s}{m_{max}}. \tag{16}$$

The maximum modulation index m_{max} is determined according to the switching frequency and minimum on-time and dead-time of the IGBTs switching [20]. According to [28], the optimum values for switching frequency for DSCC MMC with phase-shift modulation is 2.5 times or 4 times the line frequency. The first value results in minimum losses, while the second value results in better dynamic performance. Therefore, considering a system with 60 Hz, the switching frequency of 240 Hz is employed in order to obtain faster dynamic response and better individual balancing. Considering 1.5 μs for the minimum on-time and dead-time, the maximum modulation index is 0.9993. Therefore, the approximate value of the effective dc-link voltage is $v_{dc} = 33$ kV.

The number of SMs is determined by:

$$N = \frac{1}{f_{us}} \frac{v_{dc}}{V_{svc}}, \tag{17}$$

where f_{us} is defined by the ratio between the nominal voltage of SMs v_{sm} and semiconductor device voltage class V_{svc}. Literature suggests that semiconductor devices cannot operate with voltages larger than 60 % of V_{svc}.

Furthermore, the number of redundant SMs per arm is given by:

$$M = f_r N, \tag{18}$$

where f_r is the redundancy factor. This factor is a compromise between reliable operation and costs. In most works of literature, a redundancy factor around 10 % is employed [5],

[6]. For RAS, RASO and RSS, this means that the number of SM is increased in 10 %. For SR, this means that even if 10 % of SMs fails the voltage of the operating SMs is increased, avoiding overmodulation.

It is important to note that the number of spare SMs is equal to M in order to obtain the same f_r. Assuming that the SMs voltage can oscillate with 10 % of ripple, $f_{us} = 0.5$ is generally employed. This assumption is valid for both RAS and RSS, where v_{sm} is essentially constant. For RASO, the SM operates with reduced voltage and $f_{us} = 0.5$ is sufficient. However, for SR strategy, v_{sm} increases when failures happen. In this case, the following relation can be found for f_r and f_{us}:

$$f_r = 1 - \frac{f_{us,0}}{f_{us,f}}. \tag{19}$$

where $f_{us,0}$ is the utilization factor in normal conditions and $f_{us,f}$ is the utilization factor when all admissible failures happen. According to (19), if the required redundancy factor is 10 %, the utilization factor of semiconductors for SR strategy increases from $f_{us,0} = 50$ % to approximately $f_{us,f} = 56$ %.

Therefore, considering semiconductors with voltage class of 3.3 kV, $N = 20$ and $M = 2$ are obtained for both RAS, RASO and RSS strategies. In RAS and RASO, all 22 SMs are operating. For RSS strategy, 20 SMs are operating, while 2 are spare SMs. Finally, for SR strategy, $N = 20$ is employed and all of them are operating.

B. Semiconductor devices

In order to define the current of the semiconductor devices, it is necessary to determine the expressions for the MMC STATCOM arm currents. The arm currents per phase can be expressed by:

$$\begin{cases} i_u = i_c + \dfrac{i_g}{2}, \\ i_l = i_c - \dfrac{i_g}{2}, \end{cases} \tag{20}$$

If the MMC injects both positive and negative sequence currents, i_g is given by:

$$i_g = \widehat{I}^{+} cos(\omega t + \phi^{+} + \theta_v) + \widehat{I}^{-} cos(\omega t + \phi^{-} - \theta_v), \tag{21}$$

where $\theta_v \in \{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\}$ refers to the phase angle of each phase. Considering that the harmonics in the circulating current are suppressed, their value can be given by:

$$i_c = \frac{m}{4}\widehat{I}^{+} cos(\phi^{+}) + \frac{m}{4}\widehat{I}^{-} cos(\phi^{-} + \theta_v), \tag{22}$$

where $m = 2\hat{V}/v_{dc}$ is the modulation index and $\hat{V}$ is the peak value of phase voltage. Due to symmetry, only the upper arm will be analyzed. Thereby, the maximum value of the upper arm current is given by:

$$\max(i_u) = \max(i_c) + 0.5\max(i_g). \tag{23}$$

In fact, $\max(i_g) \leq \widehat{I}_n$, which is given by:

$$\widehat{I}_n = \frac{\sqrt{2}\,S_n}{\sqrt{3}\,V_g}. \tag{24}$$

where S_n is the STATCOM nominal power. Finally, the maximum value of circulating current corresponds to $\phi^{+} = 0$ and $\phi^{-} + \theta_v = 0$ and is given by:

$$\max(i_c) = \frac{m}{4}(\widehat{I}^{+} + \widehat{I}^{-}) \leq \frac{1}{4}\widehat{I}_n. \tag{25}$$

Thereby, a superior limit for the arm currents is given by:

$$max(i_u) = \frac{3}{4}\widehat{I}_n. \tag{26}$$

Furthermore, the rms value of arm currents is given by:

$$i_{u,rms} = \frac{\sqrt{3}}{4}\widehat{I}_n. \tag{27}$$

Considering $S_n = 15$ MVA and $V_g = 13.8$ kV, $max(i_u) = 665.6$ A and $i_{u,rms} = 384.3$ A. Thereby, an ABB IGBT part number 5SND 0500N330300 of 3.3 kV-500 A is chosen for this application.

C. SM capacitance

The SM capacitance can be designed based on the energy storage requirements of the converter. According to [29], the minimum capacitance of the SMs is given by:

$$C = \frac{2NE_{nom}}{v_{dc}^2}, \tag{28}$$

where E_{nom} is the minimum value of the nominal energy storage per arm, which is given by:

$$E_{nom} = \frac{\Delta E_{max}}{k_{max}^2 - \max(\frac{n_u^2 - e_{v,u}k_{max}^2}{1-e_{v,u}})}, \tag{29}$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. Finally:

$$n_u = \frac{v_u}{v_{dc}}, \tag{30}$$

$$e_{v,u} = \frac{e_u}{\Delta E_{max}}. \tag{31}$$

The excess energy storage ΔE_{max} and the energy variation e_u must be known in order to complete the design methodology. Reference [29] presents expressions for these variables considering only positive sequence injection. This paper presents a similar methodology also including the negative sequence components. The energy storage in the MMC arm changes according to the instantaneous power which flows through the arm. Therefore, expressions for the instantaneous power of each arm are derived. For simplification, the grid voltage is assumed balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the positive sequence synthesized. In this case, the inserted voltages by upper and lower arm arm of each phase are given by:

$$\begin{cases} v_u = 0.5\left[v_{dc} - v_{dc}mcos(\omega t + \theta_v)\right], \\ v_l = 0.5\left[v_{dc} + v_{dc}mcos(\omega t + \theta_v)\right], \end{cases} \quad (32)$$

Due to symmetry, only the upper arm will be analyzed. By multiplying (20) by (32), it is possible to obtain:

$$p_u = \frac{v_{dc}\hat{I}^+}{8}[2cos(\omega t + \phi^+ + \theta_v) - mcos(2\omega t + \phi^+ + 2\theta_v) - m^2cos(\phi^+)cos(\omega t + \theta_v)] + \frac{v_{dc}\hat{I}^-}{8}[2cos(\omega t + \phi^- - \theta_v) - mcos(2\omega t + \phi^-) - m^2cos(\phi^- + \theta_v)cos(\omega t + \theta_v)], \quad (33)$$

The integration of relation (33) results in:

$$e_u = \frac{S}{12m\omega}\left[f^+ + \frac{I^-}{I^+}f^-\right], \quad (34)$$

where $S = \frac{3}{2}\hat{V}\hat{I}^+$. Finally, f^+ and f^- are given by:

$$f^+ = 4sin(\omega t + \phi^+ + \theta_v) - msin(2\omega t + \phi^+ + 2\theta_v) - 2m^2cos(\phi^+)sin(\omega t + \theta_v), \quad (35)$$

$$f^- = 4sin(\omega t + \phi^- - \theta_v) - msin(2\omega t + \phi^-) - 2m^2cos(\phi^- + \theta_v)sin(\omega t + \theta_v). \quad (36)$$

Therefore, the following conclusions can be stated:

- The storage energy variation results from the apparent power S, modulation index, positive sequence power angle ϕ^+, negative sequence power angle ϕ^- and current unbalance factor;
- When the STATCOM injects both positive and negative sequences, the different angular contributions in each term result in different stresses for each phase. Therefore, the energy storage requirements need to be analyzed for each phase;
- When the converter processes both positive and negative sequence reactive power, the energy variation is proportional to the apparent power processed by the converter

Since $\Delta E_{max} = max(e_u)$ and E_{nom} are proportional to the converter rated power, the energy storage requirements of the converter can be expressed by:

$$W_{conv} = \frac{6}{S_n}E_{nom}, \quad (37)$$

where W_{conv} is the required energy storage per MVA.

As mentioned in [29], the worst case for MMC in terms of energy requirements corresponds to $\phi^+ = \pi/2$. A similar conclusion can also be obtained for ϕ^-. Therefore, the storage energy requirement E_{nom} can be obtained for given values of $\hat{I}^+$ and $\hat{I}^-$. Considering $\hat{I}^+$ and $\hat{I}^-$ in the range of 0 to 1 pu, $m = 0.9$, $k_{max} = 1.1$ and $\phi^+ = \phi^- = \pi/2$, the Fig. 3 is obtained. It can be observed that the energy storage requirements increase with the current processed by the converter. Nevertheless, the positive and negative sequence components cannot be chosen arbitrary, since the converter current limitation cannot be exceeded. Actually, since $\phi^+ = \phi^- = \pi/2$, the capability curve of the MMC is defined by the equation:

$$\hat{I}^+ + \hat{I}^- = I_n. \quad (38)$$

Considering the capability curve, the maximum required value of W_{conv} is approximately 38.34 kJ/MVA, as observed in Fig. 3. Using this value, the SMs capacitance found is 3.5 mF. However, commercial capacitors generally present 10 % of tolerance. Therefore, $C = 3.85$ mF is employed in the case studies presented in the following sections.

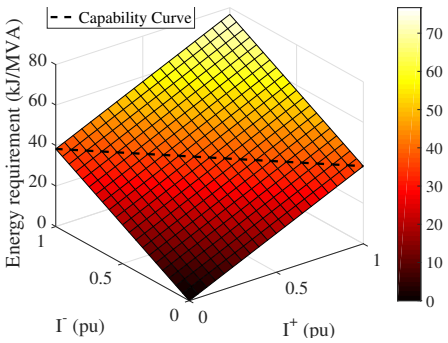

Fig. 3. Storage energy requirement for MMC considering negative sequence injection.

IV. Case Study

The performance of the redundancy strategies is evaluated for a 15 MVA MMC STATCOM whose parameters are presented in Tab. I. The parameters of the MMC controllers are shown in Tab. II. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method.

Three failure scenarios are evaluated and used for losses comparison in the case studies:

- Scenario 1: Asymmetrical failure (AS) - When the SMs of one phase fail, the other arms continue operating normally. This fact results in asymmetry in the synthesized voltage of the failed phase;
- Scenario 2: Phase symmetrical failure (PSF) - When a SM of upper arm fails, it is removed a SM from lower arm, in order to maintain the phase voltage symmetric;
- Scenario 3: Converter symmetrical failure (CSF) - When a SM of upper arm fails, the other 5 arms remove other SM, in order to maintain symmetric voltages of the converter in all phases.

Finally, the value of the SMs capacitance is inserted in the model with a tolerance of 10 % with normal distribution. Simulations are performed in PLECS environment aiming to compare the redundancy strategies in terms of dynamic behavior and power losses.

V. Dynamic Performance of Redundancy Strategies

The dynamic behavior of the redundancy strategies previously discussed are evaluated considering the injection

TABLE I
PARAMETERS OF THE MODULAR MULTILEVEL CONVERTER.

Parameter	Value
Grid voltage (v_g)	13.8 kV
pole to pole dc voltage (v_{dc})	33 kV
Rated power (S_n)	15 MVA
Transformer inductance (L_g)	1.35 mH (0.04 pu)
Transformer X/R ratio	18
Arm inductance (L_{arm})	9.4 mH (0.28 pu)
Arm resistance (R_{arm})	0.13 Ω (0.01 pu)
SM capacitance (C)	3.85 mF
SM capacitance tolerance (ΔC)	10 %
Nominal SM voltage ($v^*_{sm,n}$)	1.65 kV
Switching frequency (f_s)	240 Hz
Number of SMs (N)	20 per arm
Number of additional/spare SMs (M)	2 per arm

TABLE II
PARAMETERS OF THE CONTROLLERS.

Parameter	Value
Sampling frequency (f_a)	9.6 kHz
Prop. gain of average control ($k_{p,avg}$)	8.21
Integral gain of average control ($k_{i,avg}$)	140.7
Prop. gain of grid current control ($k_{p,g}$)	19.84
Resonant gain of grid current control ($k_{r,g}$)	1000
Prop. gain of circulating current control ($k_{p,c}$)	2.54
Resonant gain of circulating current control ($k_{r,c}$)	1000
Circulating current LPF cut-off frequency (ω_c)	8 Hz
Prop. gain of individual balancing control ($k_{p,c}$)	0.0002
Moving average filter frequency (f_m)	120 Hz

of 0.5 pu of both positive and negative sequence currents. In this condition, phase A presents the largest current peak value, since $\phi^+ = \phi^- = \pi/2$ is adopted. The results for CSF scenario are presented since its technique results in the worst transient performance in the converter.

The simulation considers the failure of one SM at 0.6 seconds and the failure of a second SM at 1.2 seconds. The objective is to explore all the converter redundancy capability. The capacitor voltages in pu of the upper arm of phase A are illustrated in Fig. 4. As observed in Fig. 4 (a), the SM voltages are balanced for RAS strategy. The reference voltage of the SMs is maintained constant, which results in smaller transient when the failures happen. The transient observed is justified by the adjustment of the carrier angular displacement, which is made dynamically according to relation (14). Additionally, the maximum value of SM voltages in steady-state does not exceed 10 %, thus validating the capacitor design.

For RASO strategy, as illustrated in Fig. 4 (b), the SMs operate with reduced voltage under normal conditions. The average voltage is 0.9 pu, resulting in an average utilization factor of $f_{us,0} = 45$ % in accordance with (19). When failures occur, the SM voltages are increased in order to maintain the effective dc-link voltage at the nominal value and avoid overmodulation. The increase in the reference voltage generates a transient response in the capacitor voltages, which reach steady-state after approximately 200 ms. When the redundancy factor is completely explored (10 % of failures = 2 SMs), the SM voltages reach the nominal value and the average utilization factor is $f_{us,f} = 50$ %.

Fig. 4 (c) illustrates the SMs voltage for RSS strategy. When the failure happens, the spare SMs are inserted and their charging process is started. During the charging process, the SM voltages reach 1.13 pu. After 230 ms, the spare SM charging process is finished and the converter reaches steady-state. It is important to observe that in RSS strategy, the number of carriers is not changed, since the failed and spare SMs are exchanged.

The results for the SR strategy are shown in Fig. 4 (d). As observed, this strategy has similar dynamic behavior to the RASO strategy. However, the SR does not present redundant SMs. Thereby, the SM voltages increase to values higher than the nominal. Considering 10 % of failures, i.e. 18 SMs operating, the average SM voltage reaches approximately 1.12 pu, resulting in a utilization factor of $f_{us,f} \approx 56$ %, in accordance with (19). Considering the voltage ripple, the maximum voltage reached is 1.2 pu in steady-state, leading to a maximum utilization factor of 60 %.

Figs. 4 (e)-(h) present the detail in the SM voltages at 1.5 seconds. As observed, even considering 10 % of tolerance in SM capacitances, the capacitor voltages in steady-state are well balanced for all strategies and the ripple remains in the 10 % range assumed in the capacitance design methodology.

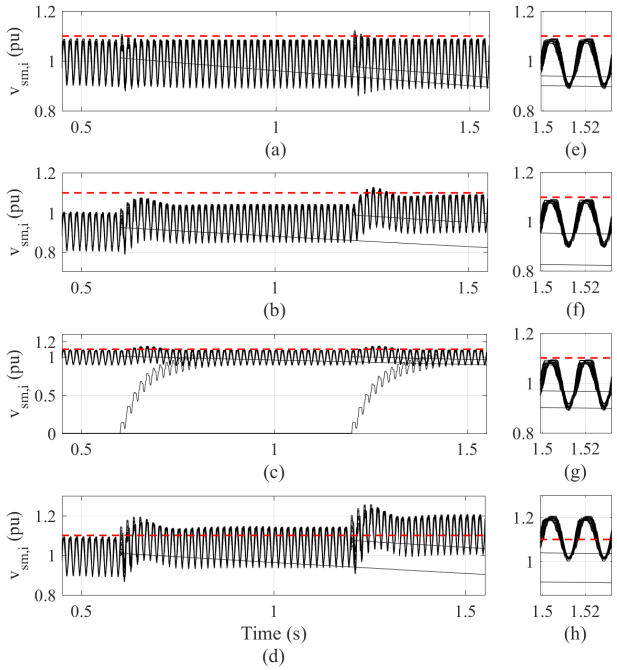

Fig. 4. Effect of the redundancy strategies in the dynamic of the SM voltages of the MMC: (a) RAS; (b) RASO; (c) RSS; (d) SR; (e) Detail for RAS strategy; (f) Detail for RASO strategy; (g) Detail for RSS strategy; (h) Detail for SR strategy.

The detail of the grid current dynamic behavior during the first failure is presented in Fig. 5. As observed in Fig. 5 (a), no significant transient is observed for RAS strategy. RASO and SR strategies present a similar performance and the current transient is rejected in approximately 140 ms, as observed in

Fig. 5 (b) and (d). Finally, Fig. 5 (c) presents the response for RSS. As observed, the transient is rejected in approximately 160 ms. Additionally, the current becomes slightly distorted. This fact is justified by the charging process of the spare SM, which increases the portion of individual action in the relations (12) and (13).

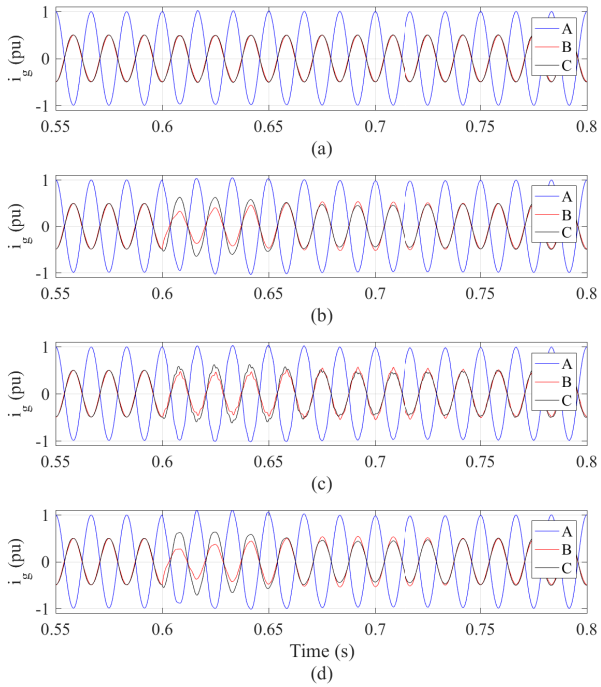

Fig. 5. Effect of the redundancy strategies in the grid current dynamic behavior: (a) RAS; (b) RASO; (c) RSS; (d) SR.

The average voltage of all SMs is presented in Fig 6. As observed, when RAS is employed, no transient is observed in the average voltage. For RSS, the average voltage presents a transient, which is rejected in approximately 200 ms. This transient is caused by the charging process of the spare SMs, which absorbs active power from the main grid. For RASO strategy, when failures happen, the average voltage is increased in order to maintain the effective dc-link voltage. Additionally, when all the redundancy factor is explored, the steady-state value of the the average voltage reaches the rated value. Finally, the transient performance of SR strategy is similar to that of RASO. Nevertheless, the SR strategy increases the average voltage to values above the nominal value. When all the redundancy margin is explored, the average voltage reaches 1.12 pu, which corresponds to the utilization factor of 56 % provided by equation (19).

Finally, considering the three failure scenarios, the power losses at the semiconductor devices of the MMC are evaluated. The obtained values are presented in Tab. III, where N_f refers to the number of failed SMs per arm. As observed, when the number of failed SMs increase, the power losses decrease, since less SMs are operating. Furthermore, Tab. III shows that the RAS strategy presents the greatest losses due to the higher number of operating SMs. The RSS hardly affects the

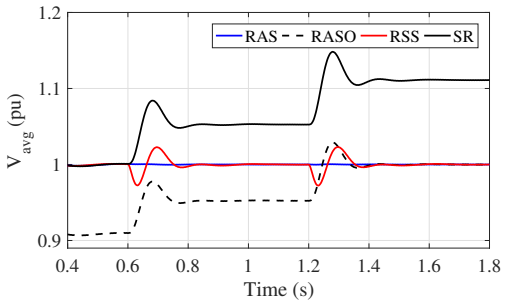

Fig. 6. Effect of the redundancy strategies in the SMs average voltage dynamic behavior: (a) RAS; (b) RASO; (c) RSS; (d) SR.

converter efficiency, since the MMC always operates with the same number of SMs. Interestingly, even with the increased SM voltages in the SR strategy, the power losses decrease, since the converter operates with fewer SMs.

TABLE III
POWER LOSSES IN THE SEMICONDUCTORS CONSIDERING THE TYPE OF FAILURE AND THE NUMBER OF FAILED SMS.

Strategy	N_f	AF (kW)	PSF (kW)	CSF (kW)
RAS	0	76.26	76.41	76.32
	1	74.80	75.39	73.35
	2	73.55	72.85	69.82
RASO	0	74.07	74.05	74.07
	1	73.48	73.25	71.83
	2	71.25	71.27	69.28
RSS	0	69.91	70.01	70.07
	1	69.68	69.84	69.91
	2	69.75	69.81	69.81
SR	0	70.02	69.72	70.02
	1	68.03	68.20	67.72
	2	66.75	66.94	64.42

As observed in previous results, RAS strategy presents a superior performance for both SM capacitor voltage dynamics and grid current control. However, this strategy presents larger power losses. These losses are slightly reduced if the RASO strategy is employed. Furthermore, these strategies present similar costs. In terms of control complexity, both RAS and RASO strategies present $12(N+M)$gate signals and the phase displacements of the carriers need to be adaptive.

The RASO and SR strategies presented similar overshoot and settling time for voltage control. The settling time for grid current is also similar. The SR presented lower losses than RASO, even working with larger voltages. This fact can be justified by the small switching frequency employed. In such condition, the conduction losses are predominant. Once the SR strategy operates with a smaller number of SMs, its power losses are reduced. This strategy also presents the smaller cost, since no additional SMs are necessary. In terms of control complexity, SR strategy presents $12N$ gate signals and the phase displacements of the carriers also need to be adaptive.

The RSS strategy presented a worst dynamic performance in terms of voltage, once the spare SMs are maintained discharged. However, this strategy considerably reduces the power losses in the MMC. This strategy has similar cost

if compared with RASO strategy. However, the control complexity is reduced, once RSS strategy presents $12N$ gate signals. Furthermore, this strategy is less complex than SR strategy, since the phase displacement of the carriers does not need to be adaptive.

It can be observed that more than one redundancy strategy can be explored in order to obtain a given redundancy factor with reduced cost. However, this discussion is beyond the scope of this work and should be addressed in further studies.

VI. Conclusions

This work presented approaches to explore the redundancy capability of MMC. Four strategies are defined and their performances are evaluated through a case study based on a 15 MVA MMC STATCOM. The presented design methodology discusses the effect of the redundancy factor and the utilization factors of semiconductors in the number of SMs. The current of the semiconductors was defined by means of the theoretical maximum value of the arm currents. Furthermore, a new design methodology for the SM capacitance was proposed, including the effect of the negative sequence current in the converter storage energy variations.

RAS strategy presents the best performance in terms of dynamic behavior but the worst performance in terms of power losses, since this technique operates with a larger number of SMs. In this context, RASO strategy results in lower power losses. However, this strategy affects the MMC dynamic behavior. RSS strategy results in the worst performance for dynamic behavior, since the charging process of the spare SMs affects the SMs voltage and grid current. Finally, SR strategy presents similar results if compared with RASO strategy. Additionally, SR strategy presents lower losses and cost (since additional SMs does not need to be included). However, this strategy increases the voltage stresses in the semiconductors and its utilization is limited to low redundancy factors.

Tab. IV summarizes the main characteristics of the studied redundancy strategies. The qualitative terms excellent, good and regular indicate the best, average and worst performance, respectively.

TABLE IV
Comparison of the redundancy strategies applied in MMC.

Strategy	RAS	RASO	RSS	SR
v_{sm} dynamics	Excellent	Good	Regular	Good
i_g dynamics	Excellent	Good	Regular	Good
Losses	Regular	Good	Excellent	Excellent
Control complexity	Regular	Regular	Excellent	Good
Cost	Regular	Regular	Regular	Excellent

VII. Acknowledgment

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