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DSCC-MMC STATCOM Main Circuit Parameters Design considering Positive and Negative Sequence Compensation

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Abstract The double-star chopper cell modular multilevel converter (DSCC-MMC) has been employed in several applications as HVDC, energy storage, renewable energy, electrical drives and STATCOMs. Generally, the DSCC-MMC main circuit parameter design presented in literature considers balanced currents flowing through the converter. Nevertheless, in STATCOM application, the converter can compensate negative sequence components and unbalanced currents flow through the DSCC-MMC, resulting in different stresses in the converter phases. Therefore, this work presents a detailed design methodology of the DSCC-MMC main circuit parameters, considering both positive and negative sequence current compensation. The dc-link voltage, number of submodules, power semiconductor thermal stresses, submodule capacitance and arm inductances are designed. Expressions for the energy storage requirements are derived when negative sequence is compensated. A case study considering a 15 MVA STATCOM is presented and simulation results validate the proposed design methodology. Finally, the converter power losses and thermal stresses in the power semiconductors are evaluated.

Keywords Modular Multilevel Converter · Static Synchronous Compensator · Negative Sequence Compensation.

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1 Introduction

In recent years, power quality issues arise the modern medium voltage (MV) distribution systems due to the high penetration of nonlinear and unbalanced loads (single-phase ac traction systems, MV motor drive systems, arc furnaces, etc.). These loads can lead to current distortions, uncontrollable reactive power, unbalances and voltage flicker (Du and Liu, 2013). Additionally, the massive penetration of renewable energy systems in the power system has led to the emergence of studies on static synchronous compensators (STATCOM) (Du and Liu, 2013; Ota et al, 2015; Mohammadi and Bina, 2011). In this context, STATCOM has an important role in the power system in terms of grid voltage regulation and reactive power control, once it can provide precise and flexible control to mitigate disturbances and effectively improve the grid power quality.

Among the various converter topologies proposed in literature, the Modular Multilevel Converter (MMC) is considered the next generation of converter for medium and high voltage STATCOMs (Tsolaridis et al, 2016). The concept of MMC consists in obtaining a high voltage converter by means of a cascade connection of converters with smaller voltage (known as cells or submodules - SMs). According to Akagi (2011), the MMC family is usually classified into four topologies:

– Single-Star Bridge Cell (SSBC);

– Single-Delta Bridge Cell (SDBC);
– Double-Star Chopper Cell (DSCC);
– Double-Star Bridge Cell (DSBC).

Generally, the DSBC-MMC topology is not applied as STATCOM, once it has a higher number of power devices in comparison with the other topologies. The SSBC-MMC topology does not have circulating current and the capacitor voltage balancing during reactive power compensation is performed through zero sequence voltage. However, according to Behrouzian and Bongiorno (2017), the negative sequence control in this topology is limited by the voltage rating of the converter. Thereby, the SSBC-MMC needs to be overdesigned in terms of voltage rating. This fact makes SSBC unsuitable for STATCOM applications.

SDBC and DSCC topologies present circulating current and are the most attractive topologies for STATCOM applications (Akagi, 2011; Tsolaridis et al, 2016). However, SDBC presents some limitations during unbalanced voltage conditions (Behrouzian and Bongiorno, 2017). In fact, the circulating current of SDBC topology increases considerably towards unbalanced voltages and the converter can trip in this situation. This fact happens because the circulating current of SDBC topology presents only one degree of freedom. This limitation is not observed in DSCC topology, since the circulating current presents three degrees of freedom (Akagi, 2011). Additionally, Tsolaridis et al (2016) compare losses and cost of SDBC and DSCC topologies. This study shows that DSCC present smaller losses than SDBC topology during negative sequence compensation. Therefore, DSCC topology presents a superior performance for STATCOM application when negative sequence currents are compensated.

In order to reduce the cost of the converter and guarantee proper operation, the main parameters of the MMC circuit must be correctly designed. Among the circuit parameters, the SM capacitance (Ilves et al, 2014; Xu et al, 2016b; Fujii et al, 2005), arm inductances (Tu et al, 2010; Xu et al, 2016b) and power semiconductor specifications (Xu et al, 2016b; Tsolaridis et al, 2016) are important issues already discussed in literature. Most works consider High Voltage Direct Current (HVDC) applications, where balanced currents flow through the converter. Nevertheless, when negative sequence currents are compensated by MMC, different voltage ripples and current stresses are observed in the converter SMs.

Therefore, literature lacks a detailed design methodology of the DSCC-MMC main circuit parameters considering both positive and negative sequence current compensation. This work meet this need and provide the following contributions:

– MMC converter design considering both positive and negative sequence compensation;
– Determination of semiconductor current stresses;
– Achievement of mathematical expressions for the energy storage requirements of MMC and the necessary SM capacitance, when both positive and negative sequence are compensated;
– Evaluation of power losses and thermal stresses in the converter.

All mathematical analysis are validated through a 15 MVA STATCOM injecting both positive and negative sequence reactive power into the power system. This work is outlined as follows. Section 2 presents the topology of the DSCC-MMC STATCOM and the control strategy employed. The design of the converter during positive and negative sequence compensation is also discussed. Section 3 presents the case study and the parameters of the simulated model. The obtained results are discussed in Section 4. Finally, the conclusions of this work are stated in Section 5.

2 Modular Multilevel Converter

2.1 Topology and Control Design

The DSCC-MMC STATCOM topology studied in this work is illustrated in Fig. 1. Each SM contains a capacitance C and four semiconductor switches (S_1, S_2, D_1 and D_2). The converter is connected to the main grid through a three-phase transformer with inductance L_g. Generally, there is a switch S_T in parallel with each SM, which is responsible for bypassing it in case of failures (Gemmell et al, 2008). The converter presents N SM per arm. i_u and i_l are the upper and lower arm currents, respectively.

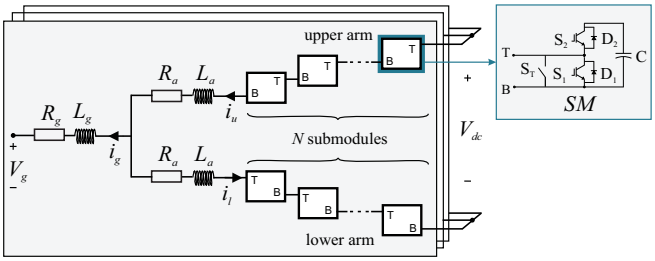

Fig. 1 Schematic of the DSCC-MMC STATCOM.

The complete control strategy for the DSCC-MMC STATCOM is presented in Fig. 2. The proposed grid current control is responsible for injecting positive and negative sequence reactive power into the grid. This strategy is performed by the inner loops, implemented in stationary ($\alpha\beta$) reference frame, resulting in a simultaneous control of positive and negative current sequences, as shown in Fig. 2 (a). Basically, the external loop controls the square of the average voltage v_{avg} of all converter SMs. Since the converter presents 6

arms, the total number of SMs is 6 N. Therefore, the average voltage is computed by:

$$v_{avg} = \frac{1}{6N}\sum_{i=1}^{6N} v_{sm,i}, \tag{1}$$

where $v_{sm,i}$ is the ith SM voltage.

The average voltage reference v^*_{avg} is given by:

$$v^*_{avg} = \frac{V_{dc}}{N}, \tag{2}$$

where V_{dc} is the nominal MMC effective dc-link voltage. Although there is no physical dc-link in DSCC-MMC STATCOM, this value is an important parameter to avoid overmodulation (Fujii et al, 2005).

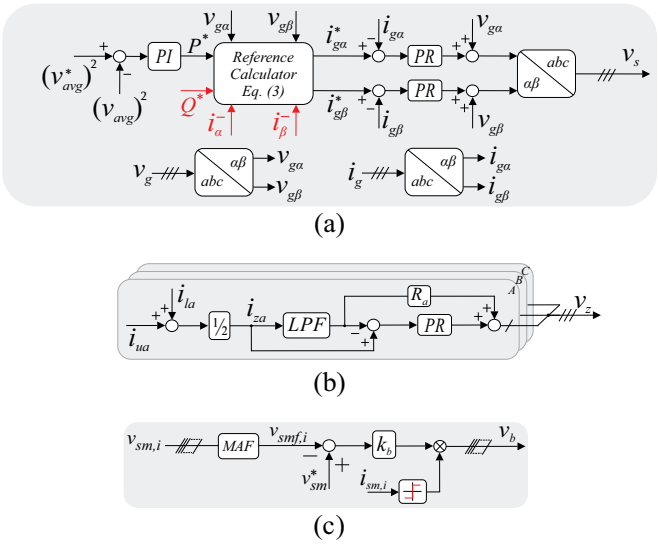

Fig. 2 Proposed control strategy for MMC-STATCOM: (a) Grid current control; (b) Circulating current control; (c) Individual balancing control.

The average voltage loop calculates the necessary active power P^* that flows to the converter. Using the instantaneous power theory (Akagi et al, 2007), it is possible to obtain expressions for the grid current reference by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{v^2_{g\alpha}+v^2_{g\beta}} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} + \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix}, \tag{3}$$

where $v_{g\alpha}$ and $v_{g\beta}$ are the stationary components of the grid voltage. The references Q^*, $i^-_{g\alpha}$ and $i^-_{g\beta}$ are dependent of the application. For example, in the case of reactive power and unbalance compensation of local loads, these values are obtained from the load current (Yue et al, 2016). In the case of voltage support or low voltage ride through (LVRT) operation, these variables are obtained through droop controllers Sharifabadi et al (2016). Nevertheless, the obtaining of these variables is out of the scope of this work and the references are directly informed to the controllers.

Two proportional resonant (PR) controllers tuned to the fundamental frequency are employed in order to track the reference current. The dynamics of the grid current in the stationary reference frame is given by (Pereira et al, 2015):

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} + L_{eq}\frac{di_{g,\alpha\beta}}{dt} + R_{eq}i_{g,\alpha\beta}, \tag{4}$$

where $L_{eq} = L_g + 0.5L_a$ and $R_{eq} = R_g + 0.5R_a$. $v_{s,\alpha\beta}$ is the equivalent output voltage of the MMC. L_a and R_a are the inductance and the resistance of the arm inductors, respectively.

Using this dynamic model, the PR controllers can be adjusted using the design methodology proposed by (Yepes et al, 2011). Feedforward actions of the grid voltage are included in order to improve the dynamic behavior.

The circulating current control is responsible for reducing the harmonics in the circulating current and inserting damping in the converter dynamic response (Harnefors et al, 2013; Moon et al, 2013). The circulating current is calculated per phase and is given by (Hagiwara and Akagi, 2009):

$$i_z = \frac{i_u + i_l}{2}. \tag{5}$$

The dynamics per phase of the circulating current per phase is given by (Harnefors et al, 2013):

$$v_z = L_a\frac{di_z}{dt} + R_a i_z, \tag{6}$$

where v_z is the STATCOM internal voltage which drives the circulating current.

Fig. 2 (b) presents the circulating current control loops. As observed, this structure is implemented per phase. Since convergence is guaranteed even without circulating current control, the circulating current reference i^*_z is obtained through low-pass filtering (LPF) of i_z (Harnefors et al, 2013). A butterworth second order filter is employed.

Regarding negative sequence injection, a considerable 2nd harmonic component appears in the circulating current (Xu et al, 2016a). This second order component generally cannot be compensated by the proportional controller (Yue et al, 2016). Therefore, three resonant controllers (one per phase) tuned to the 2nd harmonic are added to the circulating current control.

The reference voltages v_s and v_z are inputs of the modulation strategy. This paper uses the phase-shift pulse width modulation (PS-PWM) method with injection of $1/6$ of third harmonic in the phase voltages to extend the DSCC-MMC operating range (Ilves et al, 2014). The angular displacement of the carriers is calculated by the following equation:

$$\theta_{u,n} = \pi\left(\frac{n-1}{N}\right) \quad and \quad \theta_{l,n} = \theta_{u,n} + \beta, \tag{7}$$

where $n = 1, 2, ..., N$. The angle β indicates the angular displacement between the carrier waveforms in the upper and lower arms.

The angular displacements of the carrier waveforms can be chosen in terms of the desired harmonic performance. According to (Ilves et al, 2015), two different modulation strategies can be employed. In the $(N+1)-level$ modulation, the displacing of the carrier waveforms in the lower arm should be π rad from the carrier waveforms in the upper arm, i.e. $\beta = \pi$. This modulation strategy presents relatively clean circulating current and dc-link current without high order harmonics, which may be very attractive for HVDC applications (Ilves et al, 2015). However, in STATCOM applications the ac side power quality is preferred and $(2N+1)-level$ modulation is employed. The angular displacement in this strategy is given by:

$$\beta = 0 \quad \text{, N is odd} \qquad \beta = \frac{\pi}{N} \quad \text{, N is even} \tag{8}$$

In the PS-PWM method, an extra individual balancing control loop is necessary to maintain the capacitor voltages following the reference v^*_{sm}, as illustrated in Fig. 2 (c). As suggested in (Hagiwara and Akagi, 2009), a proportional controller k_b is employed. In this case, the individual balancing control law is given by:

$$v_b = k_b(v^*_{sm} - v_{smf,i})sign(i_{sm,i}), \tag{9}$$

where $i_{sm,i}$ is the arm current of the ith SM. $v_{smf,i}$ is obtained from the individual capacitor voltages through a moving average filter (MAF). This filter is responsible for attenuating the capacitor voltage ripple, improving the individual balancing performance (Sasongko et al, 2016). In such conditions, the normalized reference signals per phase are given by:

$$\begin{aligned} v_{u,n} &= v_b + \frac{v_z}{v^*_{sm}} - \frac{v_s}{N v^*_{sm}} + \frac{1}{2}, \\ v_{l,n} &= v_b + \frac{v_z}{v^*_{sm}} + \frac{v_s}{N v^*_{sm}} + \frac{1}{2}. \end{aligned} \tag{10}$$

The switching pattern of the SMs is generated by comparing the normalized reference signals $v_{u,n}$ and $v_{l,n}$ with the phase-shifted triangular carrier waves. When the reference amplitude is above the carrier, the corresponding SM is inserted to the arm. When the reference amplitude is below the carrier, the corresponding SM is bypassed.

2.2 Switching frequency

The switching frequency is an important issue in the MMC converter design. In fact, if the switching frequency is increased, two phenomena are observed. Firstly, the power losses in the semiconductor devices increase and the overall efficiency is reduced. Secondly, the capacitor voltage balancing is easier reached. Therefore, the choose of the switching frequency is a compromise between two tasks: reduce power losses and acceptable capacitor voltage balancing.

Sasongko et al (2016) analyzes the stability of the DSCC-MMC capacitor voltage balancing for various values of carrier frequency. The presented analysis shows that the interesting values for switching frequency are 2.5 times, 3.5 times or 4 times the line frequency. The first value results in minimum losses, while the last results in better dynamic performance and capacitor voltage balancing. Nevertheless, Ilves et al (2015) show that switching frequencies integer multiple of the line frequency may cause instability in the capacitor voltage balancing. Therefore, $f_c = 210Hz$ is employed in this work.

Since the ac component included in v_{sm} works as a disturbance in the current control system, it should be eliminated by a moving-average filter. According to (Sasongko et al, 2016), the moving window time must be set to:

$$1/f_{ma} = f'_n/f_n, \tag{11}$$

where f'_n is obtained from the irreducible fraction of the carrier frequency f_c with respect to the supply frequency f_n, denoted by f'_c/f'_n.[1]

2.3 Effective dc-link voltage and number of SMs

In the case study proposed in this work, a 15 MVA STATCOM with line voltage of 13.8 kV at the point of common coupling (PCC) is considered. The first step in the MMC design is the definition of the effective dc-link voltage V_{dc}. The following considerations are assumed:

- The variations in the grid voltage ΔV_g are assumed 5 %;
- The STATCOM output impedance in pu ($X_{eq} = X_g + 0.5X_{arm}$) is considered 14 % with a variation of 5 % around this value;
- The effective dc-link voltage presents in the worst case 10 % of ripple and a constant error of 3 % in steady-state.

Under these conditions, the line voltage synthesized by the STATCOM V_s is given by (Fujii et al, 2005):

$$V_s = (1+\Delta V_g)[1+X_{eq}(1+\Delta X_{eq})]V_g \approx 1.2V_g, \tag{12}$$

where V_g is the PCC line voltage.

The maximum modulation index is determined according to the carrier frequency f_c and the minimum on-time and dead-time of the IGBTs switching T_d. Accordingly:

$$m_{max} = \left(\frac{1}{f_c} - 2T_d\right) f_c. \tag{13}$$

Considering $1.5\mu s$ for the minimum on-time and dead-time, the maximum modulation index is 0.9994. In order to consider other modulation strategies, the modulation gain

[1] For example, when f_c = 210 Hz and f_n = 60 Hz, f'_c/f'_n = 7/2. Therefore, $f'_c = 7$ and $f'_n = 2$. Thereby, $1/f_{ma} = 2/f_n$.

λ is included. In this case, the minimum value of dc-link voltage can be approximated by (Fujii et al, 2005):

$$V_{dc} = \frac{2\sqrt{2}}{0.87\sqrt{3}} \frac{V_s}{\lambda m_{max}}. \quad (14)$$

Considering the modulation with injection of $1/6$ of third harmonic, $\lambda = 1.15$. Therefore, the approximate value of the effective dc-link voltage is $V_{dc} = 28kV$.

The number of SMs is determined by:

$$N = \frac{1}{f_{us}} \frac{V_{dc}}{V_{svc}}, \quad (15)$$

where f_{us} is defined by the ratio between the reference voltage of SMs v^*_{sm} and semiconductor device voltage class V_{svc}. Literature suggests that semiconductor devices cannot operate with voltages above 60 % of V_{svc}. Since the capacitor voltages presents ripple, the instantaneous value of SM voltage oscillates around the reference value v^*_{sm} and $0.45 \leq f_{us} \leq 0.5$ is employed in literature. Therefore, $f_{us} = 0.475$ is employed in this work.

Thereby, considering semiconductors with voltage class of 3.3 kV, $N = 18$ is obtained.

2.4 Semiconductor devices

In order to define the current of the semiconductor devices, it is necessary to determine the expressions for the MMC STATCOM arm currents. The arm currents per phase can be expressed by:

$$\begin{aligned} i_u &= i_z + \frac{i_g}{2}, \\ i_l &= i_z - \frac{i_g}{2}. \end{aligned} \quad (16)$$

If the MMC injects both positive and negative sequence currents, i_g is given by:

$$i_g = \widehat{I}^+ cos(\omega_n t + \varphi^+ + \theta_v) + \widehat{I}^- cos(\omega_n t + \varphi^- - \theta_v), \quad (17)$$

where $\theta_v \in \{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\}$ refers to the phase angle of each phase. $\widehat{I}^+$ and $\widehat{I}^-$ are the amplitudes of positive and negative sequence currents, respectively. ω_n is the grid frequency and φ^+ and φ^- are the positive and negative sequence current angles, respectively.

Considering that the harmonic components in circulating current are suppressed, i_z is given by (Yue et al, 2016):

$$i_z = \frac{m}{4}\widehat{I}^+ cos(\varphi^+) + \frac{m}{4}\widehat{I}^- cos(\varphi^- + \theta_v), \quad (18)$$

where m is the modulation index. Due to symmetry, only the upper arm will be analyzed. Thereby, the maximum value of the upper arm current is given by:

$$\max(i_u) = \max(i_z) + 0.5\max(i_g). \quad (19)$$

In fact, $\max(i_g) \leq \widehat{I}_n$, which is given by:

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}} \frac{S_n}{V_g}, \quad (20)$$

where I_n is the grid current peak value at nominal condition and S_n is the STATCOM nominal power. Finally, the maximum value of circulating current corresponds to $\varphi^+ = 0$ and $\varphi^- + \theta_v = 0$ and is given by:

$$\max(i_c) = \frac{m}{4}(\widehat{I}^+ + \widehat{I}^-) \leq \frac{m}{4}\widehat{I}_n. \quad (21)$$

Thereby, a superior limit for the arm currents is:

$$max(i_u) = \left(\frac{1}{2} + \frac{\lambda m_{max}}{4}\right)\widehat{I}_n \approx \frac{3}{4}\widehat{I}_n. \quad (22)$$

Additionally, the rms value of arm current is given by:

$$i_{u,rms} = \widehat{I}_n \sqrt{\frac{(\lambda m_{max})^2}{16} + \frac{1}{8}} \approx \frac{\sqrt{3}}{4}\widehat{I}_n. \quad (23)$$

Considering $S_n = 15MVA$, $V_g = 13.8kV$, $max(i_u) \approx 665.6A$ and $i_{u,rms} \approx 384.3A$. An ABB IGBT part number 5SND 0500N 330300 of 3.3kV-500A is chosen for this application.

2.5 SM capacitance

The SM capacitance can be designed based on the energy storage requirements of the converter. According to Ilves et al (2014), the minimum SM capacitance is given by:

$$C = \frac{2NE_{nom}}{V_{dc}^2}, \quad (24)$$

where E_{nom} is the minimum value of the nominal energy storage per arm, which is given by:

$$E_{nom} = \frac{\Delta E_{max}}{k_{max}^2 - \max(\frac{n_u^2 - e_{v,u}k_{max}^2}{1 - e_{v,u}})}, \quad (25)$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. Finally:

$$n_u = \frac{v_u}{V_{dc}}, \quad (26)$$

$$e_{v,u} = \frac{e_u}{\Delta E_{max}}. \quad (27)$$

The excess energy storage ΔE_{max} and the energy variation e_u must be known in order to complete the design methodology. Reference Ilves et al (2014) present expressions for these variables considering only positive sequence injection. This paper presents a methodology that includes the negative sequence components.

The energy storage in the MMC arm changes according to the instantaneous power flowing through the arm. Therefore, expressions for the instantaneous power of each arm

are derived. For simplification, the grid voltage is assumed balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. Due to symmetry, only upper arm is analyzed. Assuming the injection of $1/6$ of third harmonic component, the inserted voltages in the upper arm v_u can be expressed as:

$$v_u = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} m \cos(\omega_n t + \theta_v) + \frac{V_{dc}}{12} m \cos(3\omega_n t). \quad (28)$$

Furthermore, the upper arm current is given by:

$$\begin{aligned} i_u = {} & \frac{m\widehat{I}^+}{4}\cos(\varphi^+) + \frac{\widehat{I}^+}{2}\cos(\omega_n t + \varphi^+ + \theta_v) \\ & + \frac{m\widehat{I}^-}{4}\cos(\varphi^- + \theta_v) + \frac{\widehat{I}^-}{2}\cos(\omega_n t + \varphi^- - \theta_v). \end{aligned} \quad (29)$$

The energy variation in the upper arm can be expressed by:

$$e_u = \int v_u i_u dt. \quad (30)$$

Thus, energy variation in the upper arm can be obtained by performing the integration:

$$e_u = e_u^* + \frac{S_n}{12\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2u}\right], \quad (31)$$

where e_u^* is the energy variation obtained when sinusoidal modulation is employed, given by:

$$e_u^* = \frac{S_n}{12m\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{3u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{4u}\right]. \quad (32)$$

Additionally,

$$\begin{aligned} f_{1u} = {} & \frac{m}{9}\cos(\varphi^+)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^+ - \theta_v) \\ & + \frac{1}{12}\sin(4\omega_n t + \varphi^+ + \theta_v), \\ f_{2u} = {} & \frac{m}{9}\cos(\varphi^- + \theta_v)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^- + \theta_v) \\ & + \frac{1}{12}\sin(4\omega_n t + \varphi^- - \theta_v), \\ f_{3u} = {} & -2m^2\cos(\varphi^+)\sin(\omega_n t + \theta_v) \\ & - m\sin(2\omega_n t + \varphi^+ + 2\theta_v) + 4\sin(\omega_n t + \varphi^+ + \theta_v), \\ f_{4u} = {} & -2m^2\cos(\varphi^- + \theta_v)\sin(\omega_n t + \theta_v) \\ & - m\sin(2\omega_n t + \varphi^-) + 4\sin(\omega_n t + \varphi^- - \theta_v). \end{aligned} \quad (33)$$

Thereby, the following conclusions can be stated:

- The storage energy variation depends on the rated apparent power S_n, modulation index, positive sequence power angle φ^+, negative sequence power angle φ^- and per unit values of positive and negative sequence currents;
- When the STATCOM injects both positive and negative sequences, the different angular contributions caused by θ_v in (33) result in different stresses for each phase. Therefore, the energy storage requirements need to be analyzed for each phase. The phase with larger energy requirement is used to the computation of ΔE_{max}. Additionally, the most critical case depends on the angle φ^-;
- When the converter processes both positive and negative sequence reactive powers, the energy variation is proportional to the converter rated power.

Since $\Delta E_{max} = max(e_u)$ and E_{nom} are proportional to the converter rated power, the energy storage requirements of the converter can be expressed per MVA of rated power. Since the converter presents 6 arms, the total energy storage is 6 E_{nom}. Therefore, the required energy storage per MVA W_{conv} is given by:

$$W_{conv} = \frac{6}{S_n} E_{nom}. \quad (34)$$

As mentioned in Ilves et al (2014), the worst case for MMC in terms of energy requirements for sinusoidal modulation corresponds to $\varphi^+ = \pi/2$. In order to verify the effect of φ^-, W_{conv} is calculated considering $m = 1.15$, $\varphi^+ = \pi/2$ and $I^+ = 0.5$ pu for $0 \leq \varphi^- \leq 2\pi$ and $0 \leq I^- \leq 0.5pu$. The required energy storage per MVA is plotted in Fig. 3. As observed, the maximum of energy storage requirement does not happen when $\varphi^- = \pi/2$, due to the distortions inserted by the third harmonic added by the modulation strategy. However, if $\varphi^- = \pi/2$ is adopted as critical angle, the error in the energy storage requirement is less than 2%. Once the mismatch is small, $\varphi^+ = \varphi^- = \pi/2$ is adopted in the capacitance design.

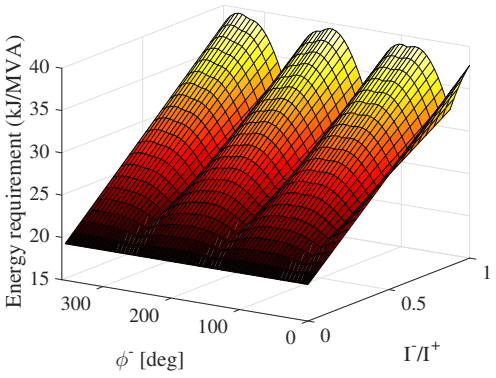

Fig. 3 Effect of the negative sequence angle φ^- on the energy storage requirements.

Finally, the energy storage requirement W_{conv} can be obtained considering $\widehat{I}^+$ and $\widehat{I}^-$ in the range of 0 to 1 pu, $m = 1.15$, $k_{max} = 1.1$ and $\varphi^+ = \varphi^- = \pi/2$. The obtained

surface is plotted in Fig. 4. It can be observed that W_{conv} increases with the current processed by the converter. Nevertheless, the positive and negative sequence components cannot be chosen arbitrarily, since the converter rated current cannot be exceeded. Actually, since $\varphi^+ = \varphi^- = \pi/2$, the capability curve of the MMC is defined by the equation:

$$\widehat{I}^+ + \widehat{I}^- = \widehat{I}_n. \tag{35}$$

Taking into account the capability curve, the maximum required value of W_{conv} is approximately 38.63 kJ/MVA, as observed in Fig. 4. Using this value, the SMs capacitance found is approximately 4.5 mF. Once $k_{max} = 1.1$, this capacitance value guarantees that the voltage ripple in steady-state is at most 10 % for any positive and negative sequence combinations under the capability curve.

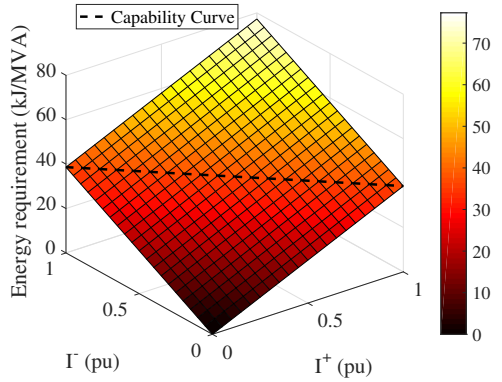

Fig. 4 Energy storage requirements as function of positive and negative sequence current components.

2.6 Arm Inductance

The arm inductance performs two important tasks for MMC STATCOM: It improves the characteristic of circulating current and it limits fault currents.

Regarding the circulating current, since the second harmonic is suppressed by the proposed control strategy, the arm inductance needs to be chosen to prevent resonance (Ilves et al, 2012). In fact, there is a resonant frequency resultant from the interaction of SM capacitances and arm inductances that must be avoided. In this case, the product of the arm inductor and the SM capacitance needs to satisfy the following relation (Ilves et al, 2012):

$$L_{arm}C > \frac{5N}{48\omega_n^2}. \tag{36}$$

Taking the most critical fault into consideration, a short circuit fault is applied between the positive and negative dc-buses. To limit the fault current, the arm inductance should satisfy (Tu et al, 2010):

$$L_{arm} = \frac{V_{dc}}{2\alpha}, \tag{37}$$

where α (kA/s) is the maximum current rise rate.

According to (37), if the maximum current rise rate is $\alpha = 0.1(kA/\mu s)$ (Xu et al, 2016b), the minimum value of arm inductance is 0.14 mH (0.004 pu). By applying (36), $L_{arm} > 2.9mH(\approx 0.09pu)$. Typically, the per unit (pu) arm inductance values for grid connected converters are limited in the range of 0.3 pu. This work employs $L_{arm} = 0.15pu$, which meets the previous criteria and reduces the high order harmonics in circulating current. Thus, $L_{arm} = 5.1mH$.

2.7 Thermal model

The junction temperature of the semiconductor devices is an important variable that directly affects the lifetime and the reliability of the converter (Sangwongwanich et al, 2016). The equivalent thermal circuit of Fig.5 is employed to observe the thermal behavior of the devices in each SM (Tu and Xu, 2011). The junction-to-case thermal impedance Z_{j-c} is modeled by a multilayer Cauer model while the case-to-heatsink thermal impedance Z_{c-h} is modeled by a thermal resistance. Both Z_{j-c} and Z_{c-h} are obtained from the datasheets. For example, the thermal parameters for the Cauer model of the ABB IGBT part number 5SND 0500N 330300 are shown in the Tab. 1.

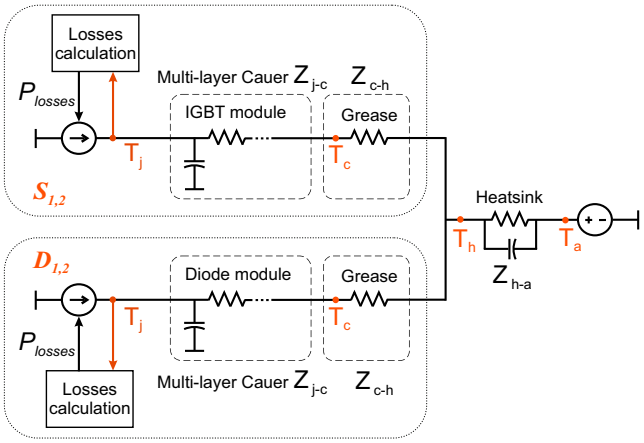

Fig. 5 Thermal model of the power devices in the half-bridge SM with a common heatsink.

In general, the heatsink and the cooling systems (which define the thermal impedance Z_{h-a}) are designed to ensure that the steady-state junction temperature T_j of the semiconductor device is within a safety limit (e.g., below 150 °C). The design procedure is based on thermal simulations. Since the heatsink-to-ambient thermal capacitance is much larger

Table 1 Parameter of the thermal model.

Device	Parameter	Z_{j-c}				Z_{c-h}
IGBT	R_i [K/W]	0.0035	0.005	0.0069	0.010	0.024
	C_i [J/K]	0.5941	2.156	4.279	11.02	-
Diode	R_i [K/W]	0.0071	0.010	0.014	0.02	0.048
	C_i [J/K]	0.2933	1.063	2.104	5.727	-

than the power module thermal capacitances, this variable is frequently disregarded, resulting in faster thermal simulations (Tu and Xu, 2011).

Considering the ambient temperature as T_a and the maximum heatsink temperature as $T_{h,max}$, the heatsink-to-ambient thermal resistance can be approximated by:

$$R_{h-a} = 6N\frac{T_{h,max} - T_a}{P_{lt}}, \tag{38}$$

where P_{lt} are the total power losses of the MMC in the worst operational case.

Power losses are estimated through the model proposed by (Smirnova et al, 2014). The conduction and switching losses are obtained from look-up tables based on the data provided in datasheets (Smirnova et al, 2014). The estimated junction temperature is used in the calculation of losses. The power losses of each device are then fed back to the thermal model, similarly to proposal in (Tu and Xu, 2011) and illustrated in Fig. 5.

Considering $T_a = 40\,^{\circ}\text{C}$, $T_{h,max} = 80\,^{\circ}\text{C}$ in the worst case and P_{lt} as 0.5 % of rated power, $R_{h-a} = 0.05K/W$ is obtained.

3 Case Study

The main circuit parameters of the designed DSCC-MMC STATCOM are presented in Tab. 2. The controller parameters are shown in Tab. 3. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method.

Table 2 Parameters of the modular multilevel converter.

Parameter	Value
Grid voltage (v_g)	$13.8kV$
Line frequency (f_n)	$60Hz$
pole to pole dc voltage (V_{dc})	$28kV$
Rated power (S_n)	$15MVA$
Transformer inductance (L_g)	$1.35mH(0.04pu)$
Transformer X/R ratio	18
Arm inductance (L_{arm})	$5.1mH(0.15pu)$
Arm resistance (R_{arm})	$0.065\Omega(0.005pu)$
SM capacitance (C)	$4.5mF$
Nominal SM voltage ($v^*_{sm,n}$)	$1.56kV$
Carrier frequency (f_c)	$210Hz$
Number of SMs (N)	18 per arm

Table 3 Parameters of the controllers.

Parameter	Value
Sampling frequency ($f_a = 2Nf_c$)	$7.56kHz$
Proportional gain of average control ($k_{p,avg}$)	8.39
Integral gain of average control ($k_{i,avg}$)	143.9
Proportional gain of grid current control ($k_{p,g}$)	6.3
Resonant gain of grid current control ($k_{r,g}$)	1000
Proportional gain of circulating current control ($k_{p,c}$)	1.3
Resonant gain of circulating current control ($k_{r,c}$)	1000
Circulating current LPF cut-off frequency (ω_c)	$8Hz$
Proportional gain of individual balancing control ($k_{p,c}$)	0.0004
Moving average filter frequency (f_{ma})	$30Hz$

The case study considers three operational conditions:

- $0 \leq t \leq 0.2$ seconds: The MMC STATCOM injects 1 pu of positive sequence reactive power into the power grid;
- $0.2 < t \leq 0.6$ seconds: The MMC STATCOM injects 0.5 pu of positive sequence reactive power and 0.5 pu of negative sequence reactive power into the power grid;
- $0.6 < t \leq 1$ seconds: The MMC STATCOM injects 1 pu of negative sequence reactive power into the power grid.

Simulations are performed in PLECS environment aiming to validate the design methodology proposed. Power losses and thermal stresses in the SM power modules are also evaluated.

4 Results

Fig. 6 illustrates the instantaneous active and reactive power injected into the power system. As observed, at $t = 0.2s$ the STATCOM injects 0.5 pu of negative sequence added to 0.5 pu of positive sequence. Thereby, the instantaneous active and reactive power present oscillatory components at the doubled line frequency (120 Hz). The instantaneous active power presents an average value that supplies the power losses of the converter.

Similar phenomena can be observed at $t = 0.6s$, when the STATCOM injects 1 pu of negative sequence. However, the amplitude of oscillatory component increases, since more negative sequence is injected. Regarding the time response, the system reaches the steady-state approximately 250 ms after the reference step.

The instantaneous power references affects directly the injected current, as shown in Fig. 7. When the STATCOM injects 1 pu of positive sequence, the currents are balanced and similar stresses are observed in each phase of the converter. Nevertheless, when the converter processes both sequences, the currents are clearly unbalanced and therefore the stress in the phase components is different. When the STATCOM injects 1 pu of negative sequence, the currents are not balanced, since there is an amount of absorbed positive sequence due to the converter power losses.

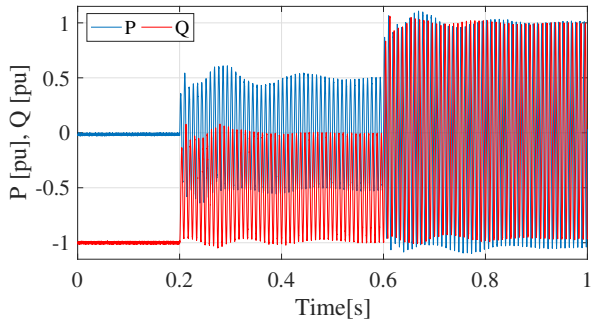

Fig. 6 Instantaneous active and reactive power injected by the MMC STATCOM.

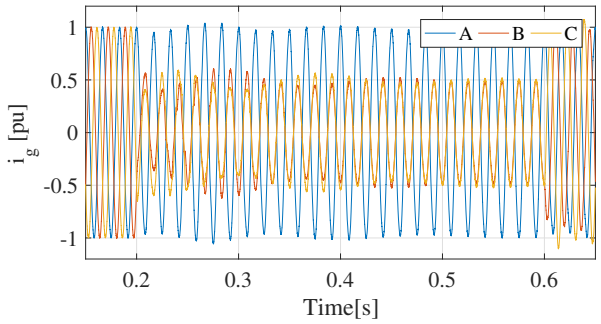

Fig. 7 Grid currents injected by the MMC STATCOM.

The SM capacitor voltages are shown in Fig. 8. Due to symmetry, only upper arms are presented. As observed, the capacitor voltages are well balanced. Furthermore, the SM voltage ripple depends on the values of positive and negative sequences, as suggested by the energy storage requirements previously analyzed. Different ripples are observed in each phase. Phase A is the most stressed, since its current is always close to 1 pu (Fig. 7). The dashed lines indicate the 10 % range adopted in the design methodology. The transient value reaches 1.16 pu in the worst case. As observed, the designed capacitance value guarantees that the maximum ripple in steady-state for the most stressed phase is within the 10 % range. Regarding the time response of the control strategy, the SM voltages reach the steady-state in approximately 300 ms.

The circulating currents of the MMC STATCOM are presented in Fig. 9. When only positive sequence is injected, the circulating currents are null, since only reactive power is injected. When negative sequence is injected, the circulating currents at legs B and C present a dc value. Furthermore, the second harmonic component is almost fully compensated by the control strategy employed. The time response of circulating currents is approximately 200 ms.

The power losses of each SM were also evaluated. Basically, the conduction and switching losses were computed for the IGBTs and for the diodes. Then, the losses per phase

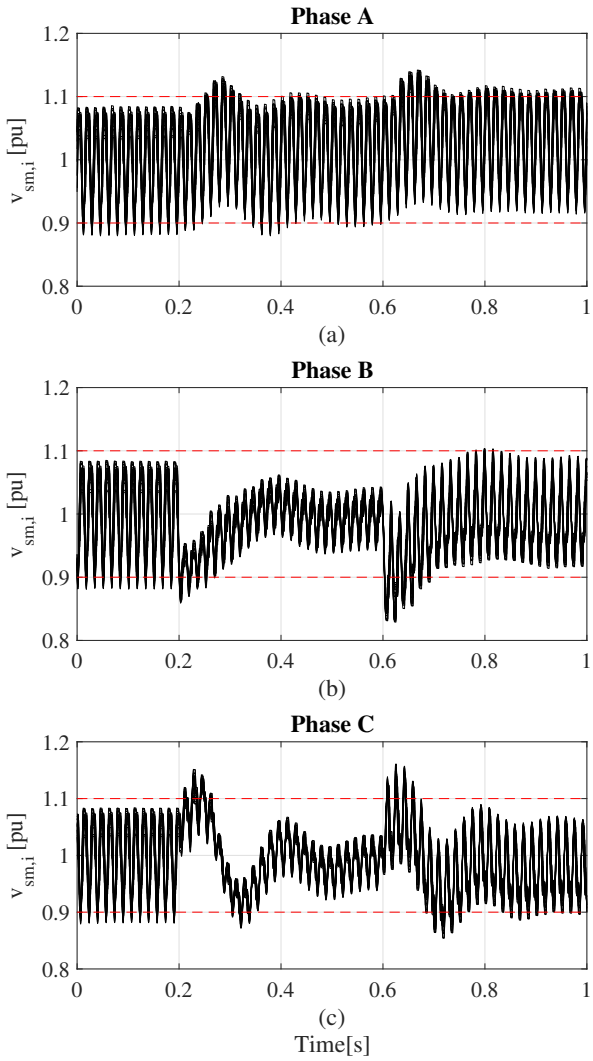

Fig. 8 SM voltages of MMC STATCOM: (a) Upper arm of phase A; (b) Upper arm of phase B; (c) Upper arm of phase C.

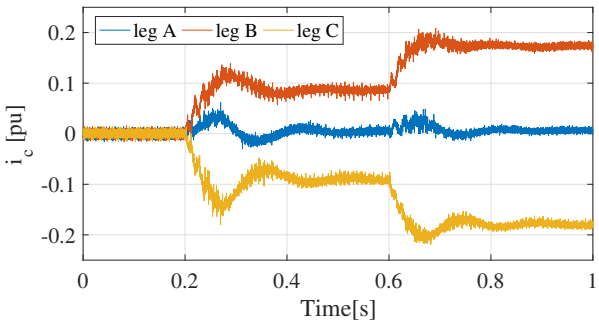

Fig. 9 Circulating currents of the MMC STATCOM.

were obtained, as shown in Tab. 4. When the converter processes only positive sequence, the losses in each phase are very similar, since the currents are balanced and the SM voltages present a similar ripple . However, when negative sequence is injected, the different current and voltage stresses

result in unbalanced power losses. Furthermore, the total losses are slightly larger than 1 pu of positive sequence when the converter processes 1 pu of negative sequence. When the converter processes 0.5 pu of each sequence, the power losses are reduced. This fact is justified by the currents at phases B and C (Fig. 7), which present smaller peak value. Thus, both conduction and switching losses are reduced.

Table 4 Power losses in the semiconductor devices.

Condition	Phase			Total (kW)
	A (kW)	B (kW)	C (kW)	
$\hat{I}^{+} = 1pu$	25.99	25.97	25.97	77.93
$\hat{I}^{+} = \hat{I}^{-} = 0.5pu$	26.25	12.56	11.07	49.89
$\hat{I}^{-} = 1pu$	26.49	31.69	26.70	84.88

Figs. 10,11 and 12 show the thermal stresses in the SM devices. Only the upper arms are presented for simplification. When positive sequence is compensated, the diodes D1 and D2 presented the largest junction temperatures, as shown in Figs. 10 (c) and (d). The junction temperatures in all 18 SMs are well balanced and remain within the safety range, since the power module employed is able to support junction temperatures until 150 °C.

When both sequences are compensated, the different current stresses affects the converter thermal balance as observed in Fig. 11. The power devices of phase A present approximately the same temperature profile, since its current stress is little affected in the case study. Phase B presented reduced junction temperature of the devices S1, D1 and D2, while Phase C experimented reduced junction temperature of the devices S1, S2 and D1. When MMC injects 1 pu of negative sequence into the grid, the thermal imbalance between the converter phases is increased, as shown in Fig. 12.

The most stressed device is diode D2 of phase C, whose maximum junction temperature reaches 110 °C, Fig. 12 (d). For the other devices, the junction temperature is always smaller than 100 °C. Furthermore, the temperature cycling amplitude due to line frequency is smaller than 7 °C for diodes and 4 °C for the IGBTs. In fact, if the power devices operate at smaller temperatures, their lifetime is considerably increased and the reliability of the MMC STATCOM is improved. However, this analysis exceeds the scope of this work.

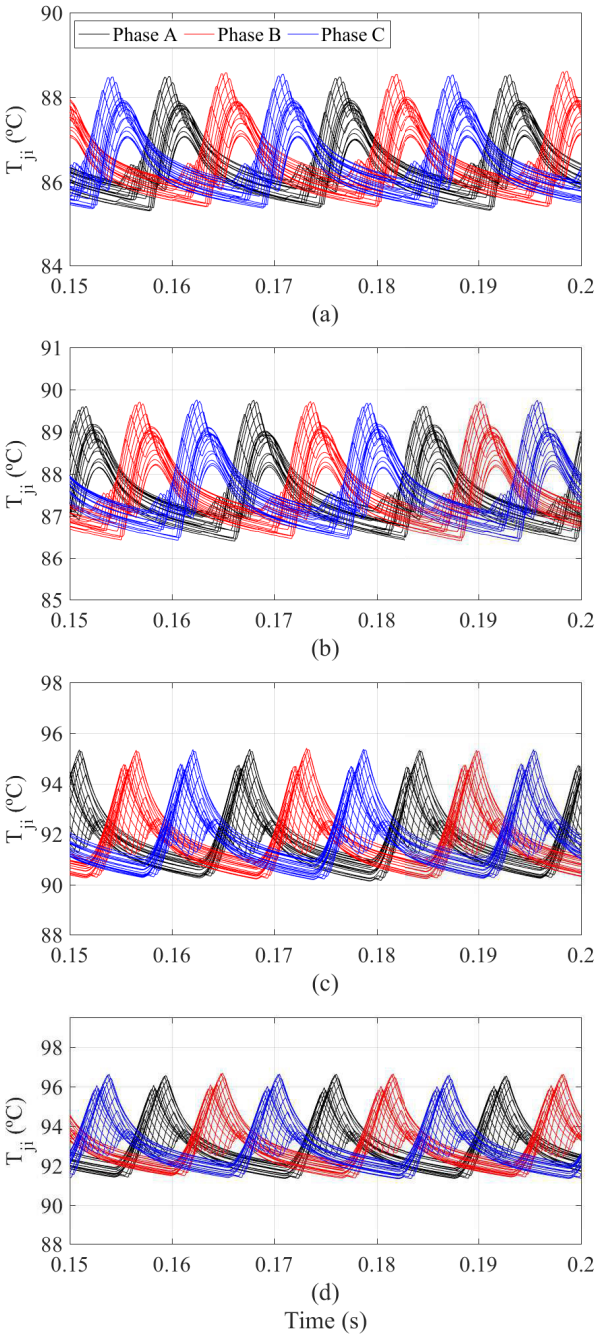

Fig. 10 Junction temperatures of the semiconductor devices considering $\hat{I}^{+} = 1pu$: (a) IGBT S1; (b) IGBT S2; (c) Diode D1; (d) Diode D2.

5 Conclusions

This work presented a detailed design methodology of the main circuit parameters of DSCC-MMC considering both positive and negative sequence current compensations. The dc-link voltage, number of SM, power semiconductor stresses, SM capacitance and arm inductances were designed for a 15 MVA MMC STATCOM.

Expressions for the energy storage requirements were derived when negative sequence was compensated. It is concluded that 46.75 kJ/MVA guarantee a voltage ripple less than 10 % when $1/6$ of third harmonic is inserted in the modulation strategy. The energy storage requirements were employed to design the SM capacitance. This methodology was validated through simulation results.

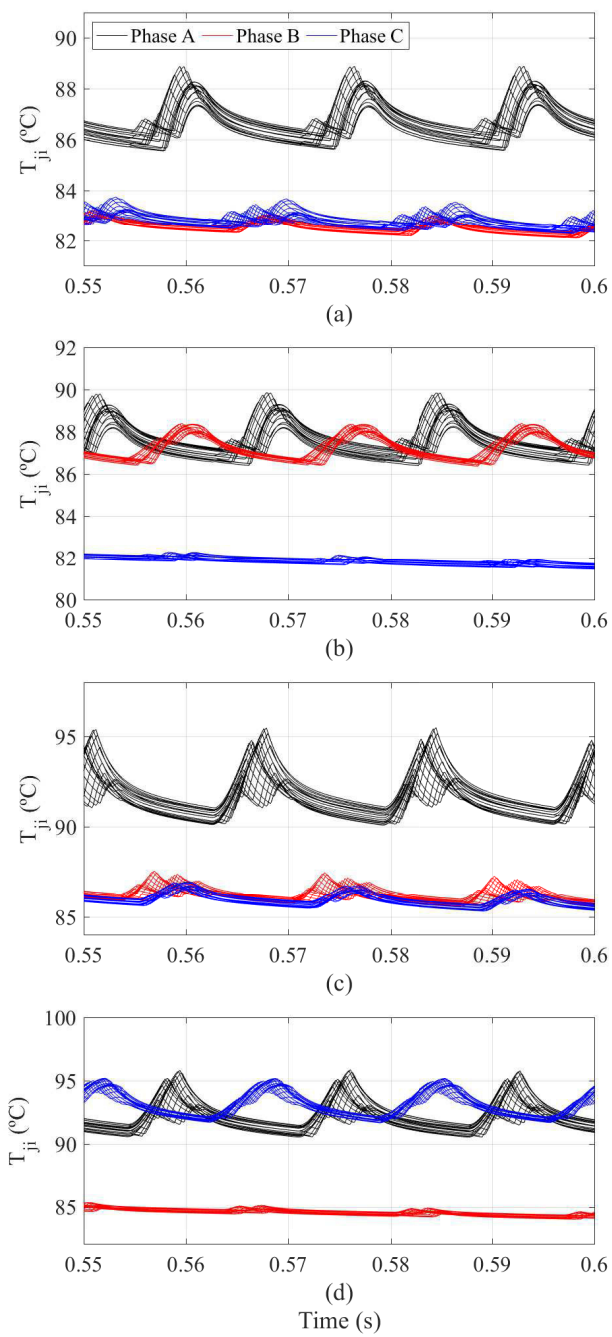

Fig. 11 Junction temperatures of the semiconductor devices considering $\widehat{I}^{+} = \widehat{I}^{-} = 0.5pu$: (a) IGBT S1; (b) IGBT S2; (c) Diode D1; (d) Diode D2.

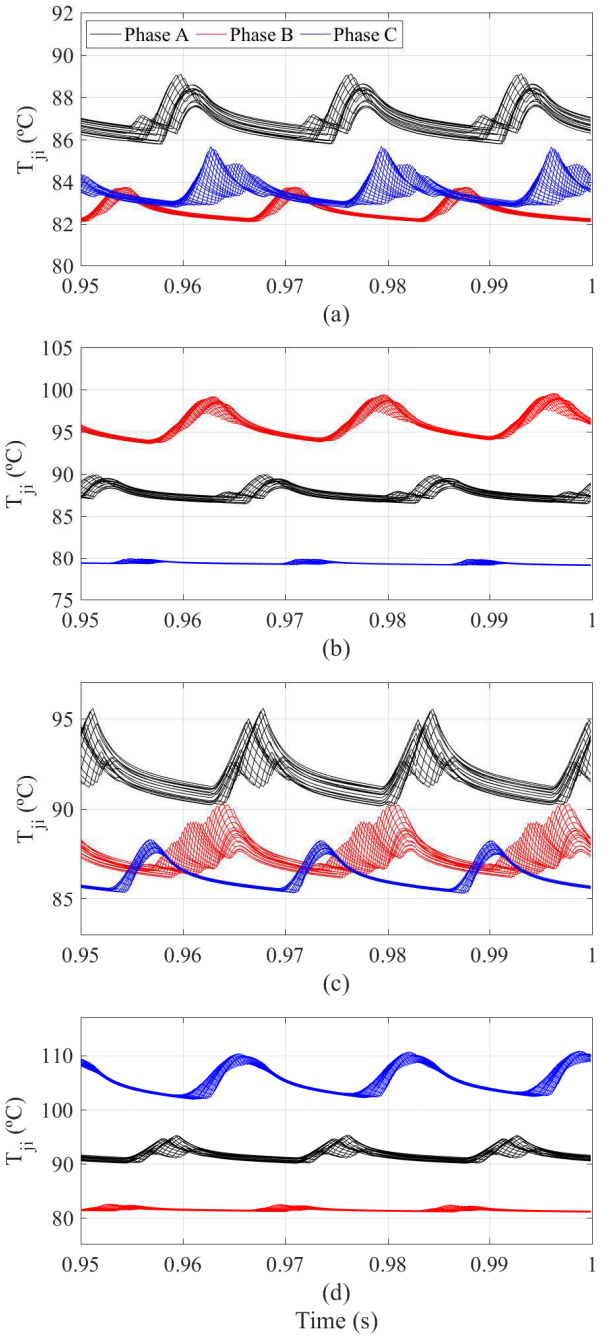

Fig. 12 Junction temperatures of the semiconductor devices considering $\widehat{I}^{-} = 1pu$: (a) IGBT S1; (b) IGBT S2; (c) Diode D1; (d) Diode D2.

A theoretical analysis of arm currents is used to define the current rating. Since the converter legs present a dc circulating current when negative sequence is compensated, one concludes that the semiconductor switches need to support more than 75 % of the converter rated current.

Additionally, the thermal design is extremely important, since the converter power semiconductor junction temperature must be within a safety limit. In this case, the heatsink-to-ambient thermal resistance was calculated using the worst case approach and validated through thermal simulations. Junction temperature values smaller than 100 °C are recommended for increasing the lifetime and consequently, the reliability of DSCC-MMC STATCOM.

6 Acknowledgment

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