GESEP – Gerência de Especialistas em Sistemas Elétricos de Potência

Título:

COMPARISON BETWEEN DOUBLE STAR TOPOLOGIES OF MODULAR MULTILEVEL CONVERTERS IN STATCOM APPLICATION

Autor:

Dayane do Carmo Mendonça

Orientador:

Prof. Dr. Heverton Augusto Pereira

Coorientador:

Eng. Renata Oliveira de Sousa

Membros:

M.Sc. Lucas Santana Xavier

Eng. João Victor Matos Farias

Aprovação:

19 de Outubro de 2018

Dayane do Carmo Mendonça

Comparison Between Double Star Topologies of Modular Multilevel Converters in STATCOM Application

Viçosa, MG

2018

Dayane do Carmo Mendonça

Comparison Between Double Star Topologies of Modular Multilevel Converters in STATCOM Application

Monografia apresentada ao Departamento de Engenharia Elétrica do Centro de Ciências Exatas e Tecnológicas da Universidade Federal de Viçosa, para a obtenção dos créditos da disciplina ELT 490 - Monografia e Seminário e cumprimento do requisito parcial para obtenção do grau de Bacharel em Engenharia Elétrica.

Orientador: Prof. Dr. Heverton Augusto Pereira

Coorientador: Eng. Renata Oliveira de Sousa

Viçosa, MG

2018

DAYANE DO CARMO MENDONÇA

COMPARISON BETWEEN DOUBLE STAR TOPOLOGIES OF MODULAR MULTILEVEL CONVERTERS IN STATCOM APPLICATION

Monografia apresentada ao Departamento de Engenharia Elétrica do Centro de Ciências Exatas e Tecnológicas da Universidade Federal de Viçosa, para a obtenção dos créditos da disciplina ELT 490 – Monografia e Seminário e cumprimento do requisito parcial para obtenção do grau de Bacharel em Engenharia Elétrica.

Trabalho aprovado em 19 de outubro de 2018.

COMISSÃO EXAMINADORA

Prof. Dr. Heverton Augusto Pereira – Orientador
Universidade Federal de Viçosa - UFV

Eng.ª Renata Oliveira de Souza – Co-orientador
Centro Federal de Educação Tecnológica – CEFET-MG

M. Sc. Lucas Santana Xavier – Membro Externo
Universidade Federal de Minas Gerais - UFMG

Eng. João Victor Matos Farias – Membro Externo
Centro Federal de Educação Tecnológica – CEFET-MG

VIÇOSA, MG
2018

À minha família, mentores e amigos.

Agradecimentos

Agradeço primeiramente a Deus pelo dom da vida e por iluminar todos os meus passos durante esta jornada. Aos meus pais, Odail e Luciana, pelo exemplo de integridade e caráter, pelo amor sem medida, incentivo, compreensão e exemplos de vida. Nos momentos mais difíceis eu lembrava que esse era o nosso sonho. PAI, MÃE, o meu muito obrigada! Ao meu irmão Arlan pela companhia, conselhos e ajuda nos estudos. Aos meus avós, tios, primos e amigos pela torcida. Àqueles que já não estão mais aqui, mas que sempre torceram por mim e continuam iluminando meu caminho de onde estiverem. Ao GESEP por toda experiência pessoal e profissional. Aos professores da graduação, especialmente ao professor Heverton, que me orientou durante este trabalho e outros estudos no GESEP. À minha coorientadora Renata e ao Allan pela paciência e ajuda no desenvolvimento desta pesquisa. Aos amigos da graduação pelo companheirismo e por toda ajuda durante esses anos.

"O sucesso nasce do querer, da determinação e persistência em se chegar a um objetivo. Mesmo não atingindo o alvo, quem busca e vence obstáculos, no mínimo fará coisas admiráveis."

(José de Alencar)

Resumo

O processo de geração, transmissão e distribuição de energia elétrica é caracterizado por complexos problemas de integração de cargas, principalmente de características não lineares. Com isso, surgiu a necessidade da criação de tecnologias de compensadores para compensação de carga e regulação de tensão. Uma dessas tecnologias de compensadores é o Compensador Estático Síncrono (STATCOM, do inglês *Static Synchronous Compensator*). Paralelamente a isso, nas últimas décadas, o uso de equipamentos de alta potência vem aumentando e tornando necessária a operação com níveis mais altos de tensão. Devido a isto, o uso de conversores convencionais torna-se inviável devido à limitação física da capacidade de tensão de bloqueio de semicondutores. Devido a esses desafios, o Conversor Modular Multinível (MMC, do inglês *Modular Multilevel Converter*) surge como alternativa para aplicações em sistemas de energia renovável, sistemas HVDC (*High Voltage Direct Current*), armazenamento de energia, acionamentos elétricos e STATCOMs. Em aplicações STATCOM, a configuração Double Star (DS) possui várias vantagens operacionais, principalmente relacionadas à sua capacidade de compensar componentes de sequência negativa e correntes desbalanceadas. No entanto, existem diversas topologias de DS. Devido a esta variedade de topologias, a contribuição deste trabalho é a comparação de duas topologias DS: Double Star Chopper-Cell (DSCC), que possui quatro dispositivos semicondutores e o Double Star Bridge-Cell (DSBC), que possui o dobro de dispositivos semicondutores em relação ao DSCC, mas apresenta capacidade de proteção em caso de um curto-circuito DC-link em uma aplicação HVDC, por exemplo. Além disso, duas variações da topologia DSBC são abordadas: DSBC-2L, que emprega modulação de 2 níveis e DSBC-3L, que emprega modulação de 3 níveis. As topologias do MMC são projetadas com base em um sistema STATCOM de 15 MVA conectado a uma rede de 13,8 kV. Essas topologias são comparadas em termos de operação em estado permanente, distorção de corrente, perdas de condução e chaveamento e viabilidade econômica. Os resultados da simulação validam a metodologia de projeto e também indicam o DSBC-3L como uma solução promissora para aplicações de média tensão.

Palavras-chaves: Conversor Modular Multinível; STATCOM; Topologias Double Star; DSCC; DSBC-2L; DSBC-3L; Estratégias de Modulação.

Abstract

The process of generation, transmission and distribution of electricity is characterized by complex problems of integration of loads, mainly of non-linear characteristics. This has led to the use of power electronic technologies for load compensation and voltage regulation. One of these technologies is the Synchronous Static Compensator (STATCOM). Moreover, in the last decades, the use of high power equipment has been increasing and requiring operation with higher voltage levels. Due to this fact, the use of conventional converters becomes infeasible due to the physical limitation of the semiconductor voltage blocking capability. Due to these challenges, Modular Multilevel Converter (MMC) comes as an alternative for applications in renewable energy systems, High Voltage Direct Current (HVDC) systems, energy storage, electrical drives and STATCOMs. In STATCOM applications, the Double Star (DS) configuration has several operating advantages, mainly related to its ability to compensate negative sequence components and unbalanced currents. However, there are many DS topologies. Due to this variety of topologies, the contribution of this work is the comparison of two DS topologies: Double Star Chopper-Cell (DSCC), which has four semiconductor devices and Double Star Bridge-Cell (DSBC), which has twice the number of semiconductor devices compared to the DSCC, however it has protection capability in case of a DC-link short circuit in an HVDC application, for example. In addition, two variations of DSBC topology are approached: DSBC-2L, which employs 2-level modulation and DSBC-3L, which employs 3-level modulation. The MMC topologies are designed based on a 15 MVA STATCOM connected to 13.8 kV grid. These topologies are compared in terms of dynamic behavior, current distortion, power losses and economic viability. The simulation results validate the design methodology and also indicates the DSBC-3L as a promising solution for medium voltage applications.

Key-words: Modular Multilevel Converter; STATCOM; Double Star Topologies; DSCC; DSBC-2L; DSBC-3L; Modulation Strategies.

List of Figures

List of Tables

List of abbreviations and acronyms

AC	Alternating Current
AVG	Average Value
BC	Bridge-Cell
CC	Chopper-Cell
DC	Direct Current
DS	Double Star
DSBC	Double Star Bridge-Cell
DSBC-2L	Double Star Bridge-Cell 2-level
DSBC-3L	Double Star Bridge-Cell 3-level
DSCC	Double Star Chopper-Cell
FACTS	Flexible AC Transmission Systems
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LPF	Low-Pass Filter
MMC	Modular Multilevel Converter
PR	Proportional Resonant
PS-PWM	Phase-Shifted Pulse Width Modulation
RMS	Root Mean Square
SDBC	Single Delta Bridge-Cell
SSBC	Single Star Bridge-Cell
SVC	Static Var Compensator
STATCOM	Static Synchronous Compensator

TDD	Total Demand Distortion
TSBC	Triple Star Bridge-Cell
VSC	Voltage Source Converter

List of symbols

V_c	Capacitor voltage
L_{arm}	Arm inductance
R_{arm}	Arm resistance
v_s	Output voltage
v_g	Point of common connection line voltage
L_g	Grid inductance
$i_{u,l}$	Arm current
$v_{u,l}$	Arm voltage
i_g	Grid current
f_c	Carrier frequency
T_d	Dead time
m_{max}	Maximum modulation index
λ	Modulation gain
v_{DC}	DC-link voltage
N	Number of cells
v_{svc}	Semiconductor device voltage class
f_{us}	Ratio between the reference cell voltage and v_{svc}
C	Cell capacitance
k_{dc}	Factor that indicates the relation between the nominal voltage of the cell and the direct voltage that is associated to the average time of energy stored in the cells
E_{nom}	Minimum value of the nominal energy storage per arm
ΔE_{max}	Excess energy storage
e_u	Energy variation

k_{max}	Upper limit of the capacitor voltages
W_{conv}	Required energy storage
S_n	Rated power
α	Maximum current rise rate
v_{avg}	Average value
v_{cell}	Cell voltage
P	Active power
Q	Reactive power
$i_{g\alpha\beta}$	Grid current stacionary frame
$v_{g\alpha\beta}$	Grid voltage stacionary frame
i_c	Circulating current
v_z	Circulating voltage
$v_{u,n}$	Reference signals for upper arm
$v_{l,n}$	Reference signals for lower arm
v_b	Individual balance voltage
$\theta_{u,n}$	Angular displacements of the upper carrier waveforms
$\theta_{l,n}$	Angular displacements of the lower carrier waveforms
β	Angular displacement between the carrier waveforms in the upper and lower arms
Z_{j-c}	Junction-to-case thermal impedance
Z_{c-h}	Case-to-heatsink thermal impedance
Z_{h-a}	Heatsink-to-ambient thermal impedance
T_j	Junction temperature
T_c	Case temperature
T_a	Ambient temperature
T_h	Heatsink temperature

P_{lt}	Total power losses
R_{h-a}	Heatsink-to-environment thermal resistance
f_g	Grid frequency
P_{switch}	Switching power
N_{semi}	Number of semiconductors devices
U_{block}	Blocking voltage
I_{nom}	Nominal current
$i_{u,rms}$	RMS value of arm current

Superscripts

$*$	Reference value
$'$	Variables for DSBC-3L

Contents

1 Introduction

The process of generation, transmission and distribution of electricity is characterized by complex problems of integration and operation (DHAL; RAJAN, 2014). In recent years, a large increase in the types of loads connected to the grid, especially those of non-linear characteristics, such as electric drive and electric arc furnace, have increased in medium voltage systems (MA; HUANG; ZHOU, 2015).

Due to this fact, the technology of thyristor valves and digital controls was initially extended to the development of Static Var Compensator (SVC) for load compensation and voltage regulation in long transmission lines in the 1970s (SINGH et al., 2009; PADIYAR, 2007). It addresses the problem of keeping steady-state and dynamic voltages within bounds, and has some ability to control stability, but none to control active power flow (KONTOS et al., 2017).

In 1988, Dr.Narain G. Hingorani introduced the concept of Flexible AC Transmission Systems (FACTS) by incorporating power electronic controllers to enhance power transfer in existing AC transmission lines, improving voltage regulation and system security without adding new lines. The FACTS controllers can also be used to regulate power flow in critical lines and hence, ease congestion in electrical networks (PADIYAR, 2007). One of the technologies in the FACTS family is the Static Synchronous Compensator (STATCOM), which can compensate positive and negative sequence reactive power (DHAL; RAJAN, 2014; MA; HUANG; ZHOU, 2015; PEREIRA et al., 2011). The STATCOM will be described in the next section.

1.1 Static Synchronous Compensator

A member of FACTS family, the STATCOM, has become a prominent device for reactive power compensation and dynamic performance improvement of the system (SHINDE; PULAVARTHI, 2017). It was developed as an advance of the SVC and applied in Voltage Source Converter (VSC) using switches such as IGBTs and GTOs. For example, a STATCOM is much more compact than a SVC for similar rating and is technically superior (PADIYAR, 2007). According to (MA; HUANG; ZHOU, 2015), STATCOM can be seen as a controllable reactive power, which can change voltage and current waveform of the inverter through power electronic means. The major attributes of STATCOM are (SINGH et al., 2009):

- Quick response time;

- Smaller footprint;
- Optimum voltage platform;
- Higher operational flexibility;
- Excellent dynamic characteristics under various operating conditions.

In the last decades, the use of high power equipments applied especially in industrial parks and large consumers, have been increasing and making operation with higher voltage levels necessary. In this context, the use of conventional converters becomes unfeasible, in particular, related to the physical limitation of the semiconductor blocking voltage capability (KONTOS et al., 2017). Due to these challenges, studies were proposed with alternative topologies, such as Modular Multilevel Converter (MMC) (CAMARGO et al., 2018; KONTOS et al., 2017; FARIAS et al., 2018). The MMC will be described in the next section.

1.2 Modular Multilevel Converter

The technology have received a lot of investiments in recent years, since it was proposed in 2001 (PEREZ et al., 2015; MARQUARDT, 2001), which led to several other studies in terms of control strategies, modulation, topologies, among others (CUPERTINO et al., 2017). This type of converter has some advantages when compared to more traditional technologies, such as VSC. The converter has been employed in several applications as High Voltage Direct Current (HVDC), energy storage, renewable energy, electrical drives and STATCOMs (AKAGI, 2011; HAGIWARA; AKAGI, 2009; ILVES et al., 2015). Among these benefits, it can mention (KONTOS et al., 2017; AKAGI, 2011):

- Modularity and scalability;
- High efficiency;
- Redundancy possibility;
- Low filtering requirements;
- High reliability;
- Lower $\frac{dv}{dt}$;
- Lower voltage stress in the power semiconductor;
- Absence of DC-link capacitors.

Furthermore, the MMC presents several construction topologies for three-phase or single phase systems, differing in relation to the type of connection and also to the type of cell. The cells are responsible for synthesizing the output voltage and can be classified according to the capacity of voltage synthesis. In traditional applications, the cells can present two or three output levels: Chopper-Cell (CC) and Bridge-Cell (BC), respectively (ZHANG; ZHAO, 2015). The Chopper and Bridge cells will be presented in the next section.

1.3 Topologies

In MMC applications, the capacity to synthesize voltage levels across the cell is linked to the capacitor voltage (V_c). Besides, the cells can present two or more output levels, depending on its construction. The most common are the Chopper-Cell and Bridge-Cell, respectively (ZHANG; ZHAO, 2015). While for the CC, the synthesis levels are restricted between 0 and $+V_c$, the BC additionally synthesizes $-V_c$ (ALLU; ODAVIC; ATALLAH, 2017).

In most of the academic works, the use of the BC is proposed due to the protection and voltage synthesis characteristics. However, some studies operate with the BC at two voltage levels (0 and V_c), as in (HE et al., 2016; ZHAO et al., 2018). On the other hand, others work with the BC operating with three voltage levels ($-V_c$, 0 and V_c), as in (HAGIWARA; AKAGI, 2009; ZHAO et al., 2018; ZHAO et al., 2017).

Regarding the classification and terminology of MMC, the references (AKAGI, 2011; KAWAMURA; HAGIWARA; AKAGI, 2014) propose the following:

- Single Star Bridge-Cell MMC (SSBC);
- Single Delta Bridge-Cell MMC (SDBC);
- Double Star Chopper-Cell MMC (DSCC);
- Double Star Bridge-Cell MMC (DSBC);
- Triple Star Bridge-Cell MMC (TSBC).

Among these topologies, the DSCC and DSBC are the most popular MMC topologies in the literature for transmission systems application. The operating characteristics of the DSBC are superior in terms of the voltage synthesis capability at the output of the converter, as well as protection capability in case of a DC-link short-circuit. Additionally, DSBC topology presents more degrees of freedom in terms of modulation. Then, the 2-level and 3-level modulation can be used (ALLU; ODAVIC; ATALLAH, 2017; LI et al., 2015). In this work, these two variations of DSBC topology are called of DSBC-2L and DSBC-3L,

respectively. On the other hand, the DSCC topology has the advantage of reduced power losses due to the smaller number of semiconductors when compared with DSBC (AKAGI, 2011). Therefore, it is necessary to carry out a study comparing these topologies.

1.4 Objectives

This work aims to make the comparison between two different Double-Star MMC topologies and two modulation variations of DSBC topology in STATCOM application: DSCC, DSBC-2L and DSBC-3L. The modulation strategies for each topology are presented, as well as the switching strategy. Thus, the specific objectives of this work are:

- Compare the operational characteristics of Double Star MMC topologies;
- Carry out a study of dynamics behavior, current distortion, power losses and economic viability for the studied topologies;
- Evaluate the control strategies for Chopper-Cell and Bridge-Cell structures in Double-Star topologies;
- Evaluate the advantages and disadvantages among the topologies studied.

1.5 Text Organization

This work is outlined as follows. Chapter 2 presents a literature review with the MMC topologies: DSCC, DSBC-2L and DSBC-3L, the control design and the modulation strategies. Chapter 3 shows the methodology which presents the case study and the parameters of the simulated model. The obtained results are discussed in Chapter 4. Finally, the conclusion of this work are stated in Chapter 5 and the continuity proposals in Chapter 6.

2 Literature Review

In this chapter, a theoretical review of the most relevant MMC concepts, such as topologies, design issues, control strategy and modulation strategies are presented.

2.1 MMC Topologies

Fig. 1 shows the MMC STATCOM topologies employed in this work, with N cells per arm. Each MMC cell contains a capacitor C, and four or eight semiconductor switches, depending of the cell types (CC or BC). The first, DSCC, is composed by four semiconductors (S_1, S_2, D_1 and D_2), as illustrated in Fig. 1(b). The second, DSBC, is composed by eight semiconductors (S_1, S_2, S_3, S_4 D_1, D_2, D_3 and D_4), as illustrated in Fig. 1(c).

The arm inductance (L_{arm}) is responsible to reduce the harmonics in the circulating current and also limiting the currents during possible faults (CUPERTINO et al., 2017). The arm resistance R_{arm} represents the copper losses of the arm inductance. However, it is not illustrated. Usually, in parallel with each cell, there is a switch S_T, which bypasses the cell in case of failures.

The choice of the Double Star topologies can be justified in terms of flexibility, in which is possible to control negative-sequence reactive power and consequently control the circulating current among the three legs of the Double Star topology (DHAL; RAJAN, 2014).

2.2 DC-Link Voltage and Number of Cells

For the MMC design, the effective DC-link v_{DC} is calculated following the considerations presented by (CUPERTINO et al., 2017). The variations in the grid voltage are assumed 5 %, the STATCOM output impedance in pu is considered 14 % with a variation of 5 % around this value and the effective DC-link presents in the worst case 10 % of ripple and a constant error of 3 % in setady-state. Therefore, according to (FUJII; SCHWARZER; DONCKER, 2005), the line voltage synthesized by the STATCOM is given by:

$$v_s \approx 1.2 v_g, \tag{2.1}$$

where v_g is the line voltage in the point of common coupling.

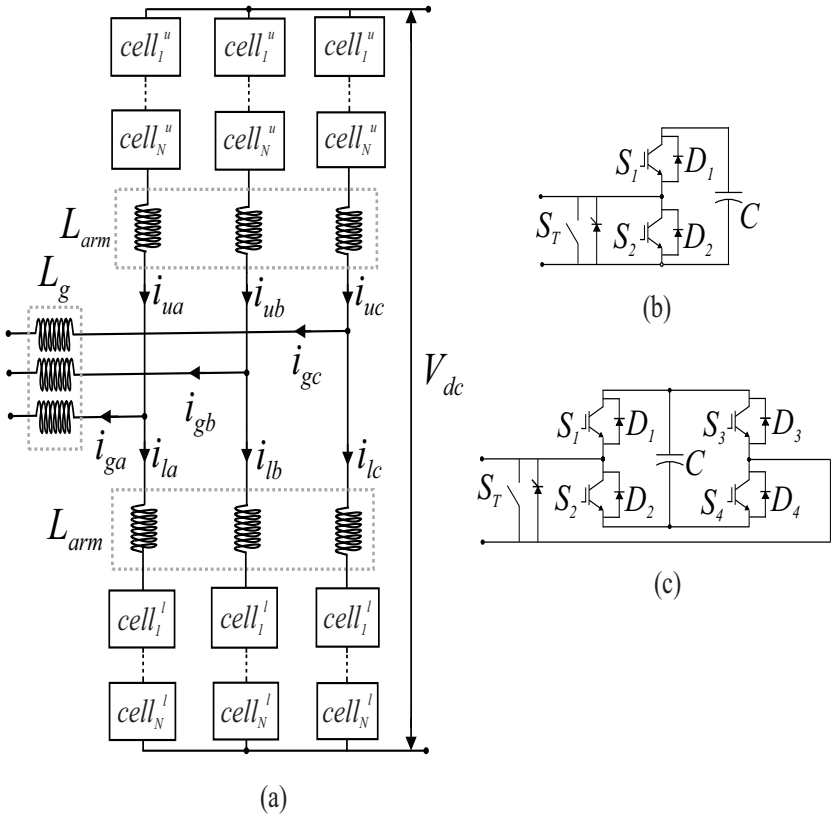

Figure 1 – Schematic of the (a) Double Star MMC topology; (b) Chopper-Cell; (c) Bridge-Cell.

In order to determine the maximum modulation index according to the carrier frequency f_c and the minimum on-time and dead time of the IGBTs switching T_d, the following is considered:

$$m_{max} = \left(\frac{1}{f_c} - 2T_d\right) f_c. \tag{2.2}$$

The carrier frequency used was 270 Hz.

For the minimum on-time and dead time, the maximum modulation index (m_{max}) is 0.99919 considering 1.5 μs. The modulation gain λ is 1.15 (CUPERTINO et al., 2017) considering the modulation with injection of 1/6 of third harmonic. In this case, the minimum value of DC-link voltage can be approximated by (FUJII; SCHWARZER; DONCKER, 2005), whereas $v_g = 13.8$ kV:

$$v_{DC} = \frac{2\sqrt{2}}{0.87\sqrt{3}} \frac{v_s}{\lambda m_{max}}. \tag{2.3}$$

Therefore, the approximate value of the minimum effective DC-link is $v_{DC} = 23$ kV. However, it was adopted the value of 25 kV, since the control of the circulating current

is not included in the DC-link voltage calculation. Besides, the number of cells can be calculated by:

$$N = \frac{1}{f_{us}} \frac{v_{DC}}{v_{svc}}, \tag{2.4}$$

where v_{svc} is the semiconductor device voltage class, f_{us} is the ratio between the reference cell voltage (v^*_{cell}) and v_{svc}. In addition, the literature suggests that semiconductor devices do not operate with voltages above 60 % of v_{svc}. Since the capacitor voltages presents ripple, the instantaneous value of cell voltage oscillates around the reference value v^*_{cell} and $0.45 \leq f_{us} \leq 0.5$ is employed. Therefore, $f_{us} = 0.475$ is considered in this work. Furthermore, considering semiconductors with voltage class of 3.3 kV, N = 16 is obtained.

2.3 Components Design: Cell Capacitance and Arm Inductance

The following design is done for DSCC and DSBC-2L, with the capacitance value being modified for the DSBC-3L, due to the value of the factor k_{dc}. This factor indicates the relation between the nominal cell voltage and the direct voltage that is associated with the time-average of the stored energy in the cells (ILVES et al., 2014). For the DSCC and DSBC-2L, the factor k_{dc} is 1.

The cell capacitance depends of the energy storage requirements of the converter and the minimum value is given by (ILVES et al., 2014):

$$C = \frac{2NE_{nom}}{k_{dc}^2 v_{DC}^2}, \tag{2.5}$$

where E_{nom} is the minimum value of the nominal energy storage per arm and is given by:

$$E_{nom} = \frac{\Delta E_{max}}{k_{max}^2 - max\left(\frac{\frac{v_u}{v_{DC}} - \frac{e_u}{\Delta E_{max}}}{1 - \frac{e_u}{\Delta E_{max}}}\right)}, \tag{2.6}$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. ΔE_{max} is the excess energy storage and e_u is the energy variation. According to (CUPERTINO et al., 2017), $\Delta E_{max} = max(e_u)$.

Since the converter presents 6 arms, the total energy storage is $6E_{nom}$ and the required energy storage per MVA is given by:

$$W_{conv} = \frac{6}{S_n} E_{nom}, \tag{2.7}$$

where S_n is the rated power with value of 15 MVA.

Thus, the maximum required value presented by (CUPERTINO et al., 2017) is 40 kJ/MVA and the cell capacitance is 5.12 mF for the DSCC.

For the calculation of the arm inductance, it is important to improve the characteristic of the circulating current and to limit the fault currents. However, in order to avoid resonance, the inductance value must satisfy the following equation (ILVES et al., 2012):

$$L_{arm}C > \frac{5N}{48w_n^2}. \tag{2.8}$$

According to (TU et al., 2010), the arm inductance necessary to limit the fault current is shown in (2.9).

$$L_{arm} = \frac{v_{DC}}{2\alpha}, \tag{2.9}$$

where α (kA/s) is the maximum current rise rate.

In the case of $\alpha = 0.1$ kA/μs, the minimum inductance value is given by 0.14 mH (0.004 pu). Also, applying (2.8), $L > 2.9$ mH (0.09 pu). Typically, the inductance values for grid connected converters are limited of 0.3 pu. Following (CUPERTINO et al., 2017), this work employs $L_{arm} = 0.15$ pu (5.1 mH), which avoid resonance, limit the fault current and reduces the high order harmonics in the circulating current.

2.4 Control Strategy

The control strategy for the Double Star MMC STATCOM is shown in Fig. 2 (ILVES et al., 2015), including the grid current control, the circulating current control and the individual balancing control. The grid current control is carried out through the derivation of components in stationary $(\alpha\beta)$ reference frame, which results in the simultaneous control of negative and positive sequence of the grid current and voltage. The control generates an output for each phase. The total number of cells is 6N, due to the presence of 6 arms in the three-phase system.

Furthermore, the outer loop controls the square of the average voltage v_{avg} of all cells of the converter. This average voltage is defined by:

$$v_{avg} = \frac{1}{6N}\sum_{i=1}^{6N} v_{cell,i}, \tag{2.10}$$

where $v_{cell,i}$ is the i-th cell voltage.

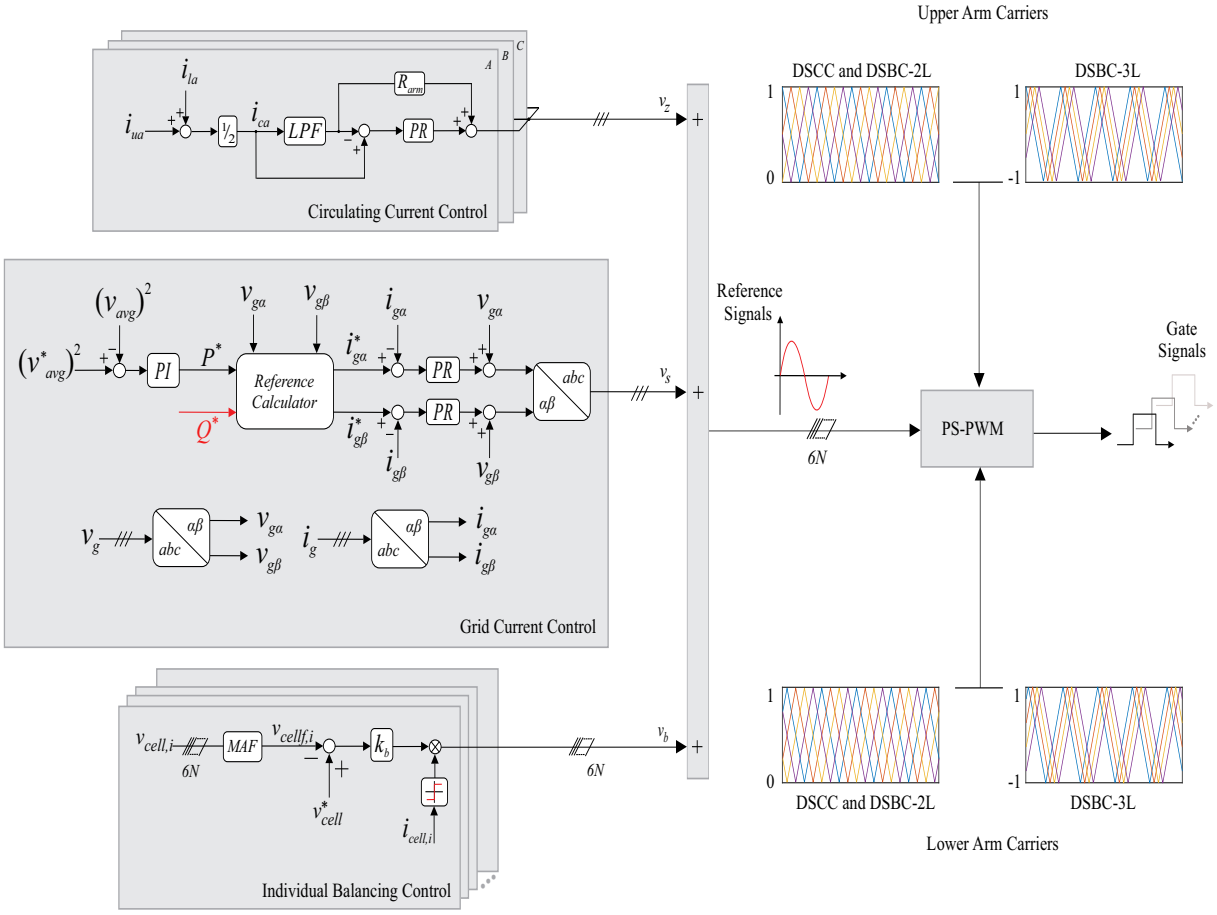

Figure 2 – Control strategy for MMC-STATCOM: circulating current, grid current and individual balancing control.

The average voltage reference v^*_{avg} and v^*_{cell} of the DSCC and the DSBC-2L are expressed by:

$$v^*_{avg} = v^*_{cell} = \frac{v_{DC}}{N}. \tag{2.11}$$

Although there is no connection on the DC-link in the DSCC-MMC STATCOM. However, this value is an important parameter to avoid overmodulation (FUJII; SCHWARZER; DONCKER, 2005).

With the equation (2.11) presented, it is possible to obtain the upper arm voltage contribution of the Chopper-Cell, as shown in Fig. 3.

Nevertheless, according to (HE et al., 2016), in order to guarantee correct operation, the capacitor voltages of the DSBC-3L must be given by:

$$v'^*_{avg} = v'^*_{cell} = \frac{1.5v'_{DC}}{N'}, \tag{2.12}$$

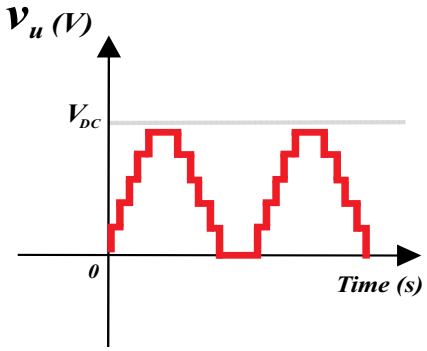

Figure 3 – Upper arm voltage for CC.

where the subscript $'$ indicates variables for DSBC-3L.

With the equation (2.12) presented, it is possible to obtain the upper arm voltage contribution of the Bridge-Cell, as shown in Fig. 4.

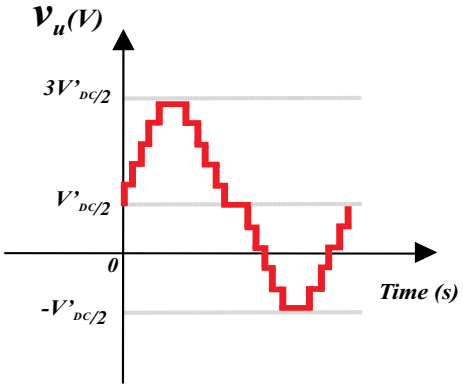

Figure 4 – Upper arm voltage for BC.

The reference calculator in Fig. 2, is used to compute the active power P^* that flows to the converter and calculate the current reference $i^*_{g\alpha}$ and $i^*_{g\beta}$. Using the instantaneous power theory (AKAGI; WATANABE; AREDES, 2007), it is possible to express the grid current, given by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = v_{g\alpha\beta} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} + \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix}, \tag{2.13}$$

where $v_{g\alpha\beta}$ is defined by:

$$v_{g\alpha\beta} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}}. \tag{2.14}$$

As for the references Q^*, $i^-_{g\alpha}$ and $i^-_{g\beta}$, in this work they are directly informed to the controllers. Also the parameters $i^-_{g\alpha}$ and $i^-_{g\beta}$ are equal to zero for all the tests performed in this work, since negative sequence injection is not performed.

The circulating current control, presented in Fig. 2, is responsible for reducing the harmonics in the circulating current and inserting damping in the converter dynamic response. The circulating current is calculated per converter leg and is given by:

$$i_c = \frac{i_u + i_l}{2}. \tag{2.15}$$

Regarding to the modulation strategy, which is dealt in Section 2.5, it is used the Phase-Shifted Pulse Width Modulation (PS-PWM). For PS-PWM method, an extra individual balancing control loop, presented in Fig. 2, is employed to maintain the capacitor voltages following the reference $v^*_{cell,j}$ (HAGIWARA; AKAGI, 2009).

The reference signals depends on the output signals, shown in Fig. 2. The normalized references to the DSCC and DSBC topologies are obtained given by (CUPERTINO et al., 2017), and expressed to:

$$v_{u,n} = v_b + \frac{v_z}{v^*_{cell}} - \frac{v_s}{N v^*_{cell}} + \frac{1}{2}, \tag{2.16}$$

$$v_{l,n} = v_b + \frac{v_z}{v^*_{cell}} + \frac{v_s}{N v^*_{cell}} + \frac{1}{2}. \tag{2.17}$$

Regarding the voltage reference, the injection of 1/6 of the third harmonic was used in order to increase the linear operational area of the modulation curve (CUPERTINO et al., 2017).

2.4.1 Relationship between cell, output and DC-link voltages

According to (THITICHAIWORAKORN; HAGIWARA; AKAGI, 2012), the term of individual balance v_b and the term of circulating voltage v_z in (2.16) and (2.17) are negligible as compared to the other two terms. As the references of the previous equations are lagged 180°, it is analyzed only for the lower arm. Therefore, $v_{l,n}$ is approximated as:

$$v_{l,n} = \frac{v_s}{N v^*_{cell}} + \frac{1}{2}. \tag{2.18}$$

2.4.1.1 DSCC

For the Chopper-Cell, the following equation should be satisfied to avoid overmodulation.

$$0 \leq \frac{1}{v^*_{cell}} \left(\frac{-v_s}{N} + \frac{V_{DC}}{2N} \right) \leq 1, \tag{2.19}$$

where v^*_{cell} is given by (2.11).

From the equation presented, the output voltage for the CC is shown in Fig. 5 and given by:

$$\frac{-v_{DC}}{2} \leq v_s \leq \frac{v_{DC}}{2}. \tag{2.20}$$

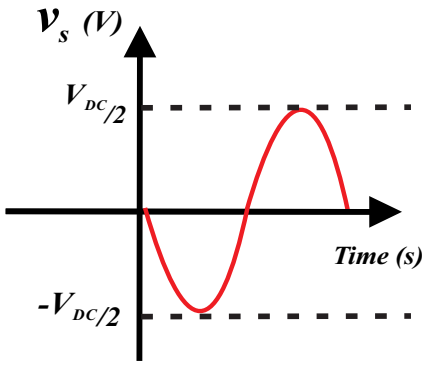

Figure 5 – Output voltage for CC.

2.4.1.2 DSBC

For the Bridge-Cell, the following equation should be satisfied to avoid overmodulation.

$$-1 \leq \frac{1}{v^*_{cell}} \left(\frac{-v_s}{N'} + \frac{V'_{DC}}{2N'} \right) \leq 1, \tag{2.21}$$

where v^*_{cell} is given by (2.12) and the subscript $'$ indicates variables for DSBC-3L.

From the equation presented, the output voltage for the BC is shown in Fig. 6 and given by:

$$-v'_{DC} \leq v_s \leq v'_{DC}. \tag{2.22}$$

2.5 Modulation Strategies

In this work, the PS-PWM modulation strategy is applied with some variations in the comparison between reference and carrier for the topologies studied. The angular displacements of the carrier waveforms can be chosen in terms of the desired harmonic performance. The angle expressed in (2.23), for DSCC and DSBC-2L, shows the existing lag

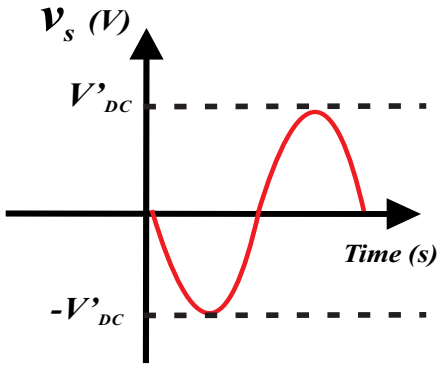

Figure 6 – Output voltage for BC.

in the upper and lower arm carriers, in turn, the β, angle indicates the angular displacement between the carrier waveforms in the upper and lower arms.

$$\theta_{u,n} = \pi(\frac{n-1}{N}) \text{ and } \theta_{l,n} = \theta_{u,n} + \beta, \tag{2.23}$$

where n = 1,2,..,N.

According to (ILVES et al., 2015), two different modulation strategies can be employed: (N + 1) level modulation, with $\beta = \pi$ and (2N + 1) level modulation, with β being presented by (2.24) and (2.25). In STATCOM applications, the AC side power quality is taken with priority. In this way the modulation level (2N + 1) is employed in the PS-PWM strategy (ILVES et al., 2015),(CUPERTINO et al., 2017).

$$\beta = \frac{\pi}{N}, \text{ if N is even,} \tag{2.24}$$

and

$$\beta = 0, \text{ if N is odd.} \tag{2.25}$$

For the DSBC-3L the angular displacements, according (LAMB; MIRAFZAL; BLAABJERG, 2018; MORA et al., 2016), can be expressed by:

$$\theta'_{u,n} = \pi(\frac{n-1}{2N}) \text{ and } \theta'_{l,n} = \theta'_{u,n} + \beta', \tag{2.26}$$

where n = 1,2,..,N and β' is defined as:

$$\beta' = \frac{\pi}{2N}, \text{ if N is even,} \tag{2.27}$$

and

$$\beta' = 0, \text{ if N is odd.} \tag{2.28}$$

2.5.1 DSCC

As observed in Fig. 1(b), it can be verified that the switches of the Chopper-Cell have two states, as is shown in Tab. 1. These states allow the voltage synthesized by each cell (v_{cell}) to be $+V_c$ or 0.

Table 1 – Switching States of the Chopper-Cell Switches.

State	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{v_{cell}}$
1	1	0	$+V_c$
2	0	1	0

Therefore, it is possible to compare the normalized voltage reference signals of the upper and lower arms with the carrier signals using PS-PWM. The comparison between normalized signals can be seen in Fig. 7. In addition, Fig. 8 exemplifies for N = 4 the reference signals, with injection of 1/6 of third harmonic, of the upper and lower arms with the $\beta = \frac{\pi}{2}$ displacement carriers. The arms voltage references presented in Fig. 8 must be between the limits shown in Fig. 3 in order to avoid overmodulation.

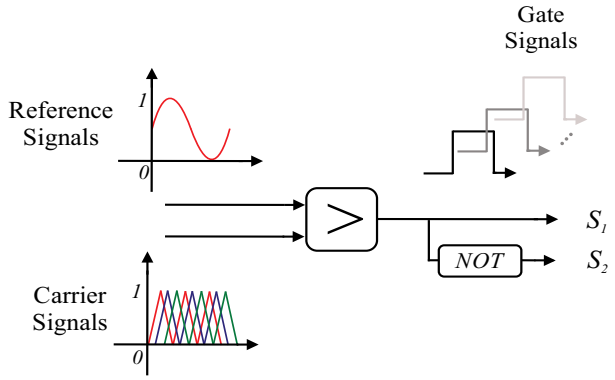

Figure 7 – PS-PWM modulation of the DSCC.

2.5.2 DSBC

As observed in Fig. 1(c), the switches of the Bridge-Cell have four states, as is shown in Tab. 2. These states allow the voltage synthesized by each cell (v_{cell}) to be $+V_c$, 0 or $-V_c$.

In the literature, some works present the DSBC-2L in which the switches work only in the first two states. For this case, the amplitude of the carriers and the references

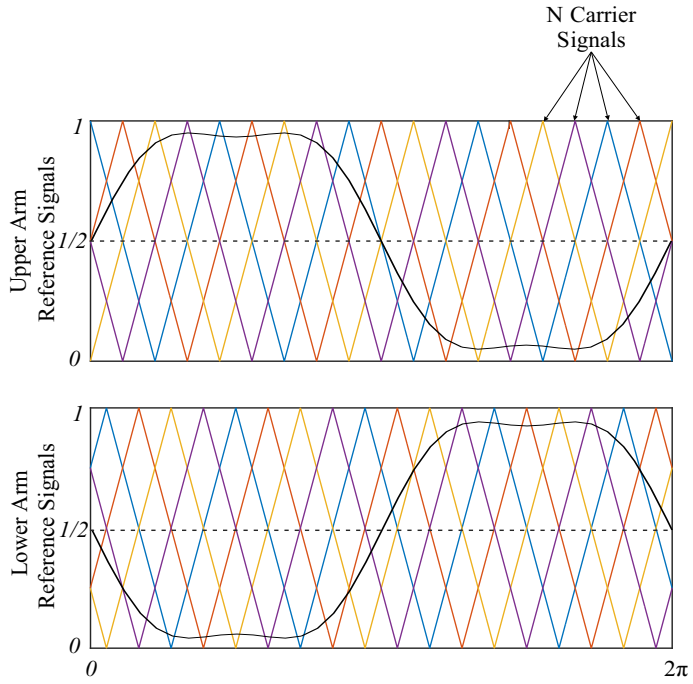

Figure 8 – Operation of PS-PWM for DSCC and DSBC-2L.

Table 2 – Switching States of the Bridge-Cell Switches.

State	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{S_3}$	$\mathbf{S_4}$	$\mathbf{v_{cell}}$
1	1	0	0	1	$+V_c$
2	0	1	0	1	0
3	1	0	1	0	0
4	0	1	1	0	$-V_c$

of the upper and lower arms are the same as in the DSCC, as in Fig. 8. The comparison between normalized signals is performed as proposed in (XIA; AYYANAR, 2017), using the unipolar modulation strategy, as illustrated in Fig. 9(a).

On the other hand, the DSBC-3L employs the four switching states, and can also synthesize the voltage $-V_c$. The comparison between normalized signals can be seen in Fig. 9(b). The unipolar modulation strategy was also used. For such comparison the carriers have amplitudes between -1 and 1, as shown in Fig. 10, for N = 4 cells per arm. The arms voltage references, with injection of 1/6 of third harmonic, presented in Fig. 10 must be between the limits shown in Fig. 4 in order to avoid overmodulation.

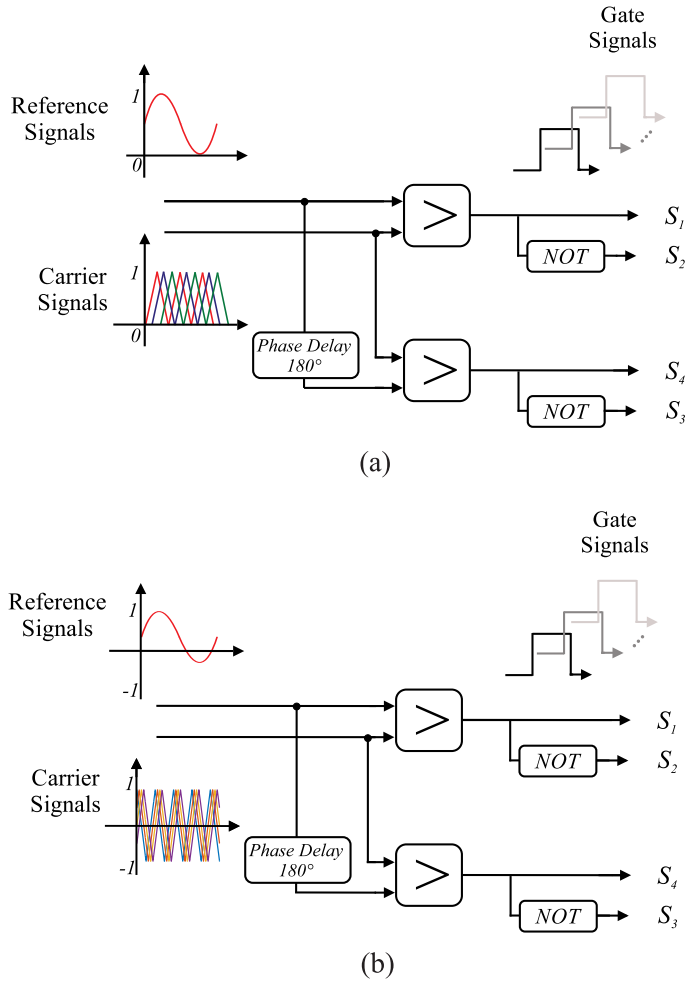

Figure 9 – PS-PWM modulation: (a) DSBC-2L; (b) DSBC-3L.

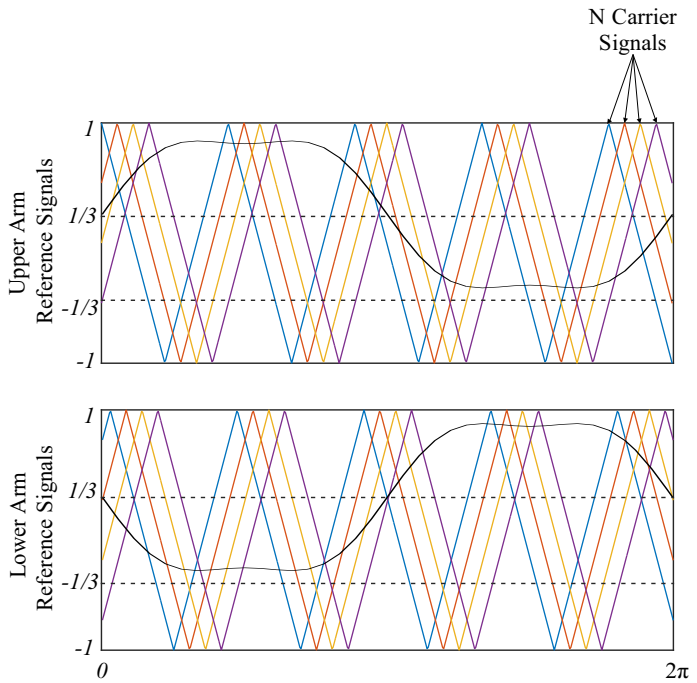

Figure 10 – Operation of PS-PWM for the DSBC-3L.

2.6 Semiconductor Devices

According to (CUPERTINO et al., 2017), an upper limit for arm currents is given by:

$$max(i_u) \approx \frac{3}{4}\widehat{I}_{nom}, \tag{2.29}$$

where $\widehat{I}_{nom}$ is given by:

$$\widehat{I}_{nom} = \frac{\sqrt{2}}{\sqrt{3}}\frac{S_n}{v_g}. \tag{2.30}$$

Additionally, the RMS value of arm current is given by (CUPERTINO et al., 2017):

$$i_{u,rms} = \frac{\sqrt{3}}{4}\widehat{I}_{nom}. \tag{2.31}$$

Considering $S_n = 15\ MVA$, $v_g = 13.8\ kV$, $max(i_u) \approx 665.6\ A$ and $i_{u,rms} \approx 384.3\ A$. An ABB IGBT part number 5SND 0500N 330300 of 3.3 kV-500 A is chosen for this application.

2.7 Thermal Model

In order to compare the thermal behavior of semiconductors in the cell, the thermal model is developed (PEREIRA et al., 2016). For the CC, the circuit of Fig. 11 is considered with a common heatsink for the two diodes and two IGBT's. Already for the BC, the circuit of Fig. 11 is duplicated, in other words, each pair of IGBT and diode is coupled to a heatsink. This is done so that the calculation of heatink resistance would remain the same for both types of cells studied.

In this context, the junction-to-case thermal impedance Z_{j-c} is modeled by a multilayer Cauer model while the case-to-heatsink thermal impedance Z_{c-h} is modeled by a thermal resistance. Both Z_{j-c} and Z_{c-h} are obtained from the datasheets (CUPERTINO et al., 2017). The thermal parameters for the Cauer model of the ABB IGBT part number 5SND 0500N 330300 are shown in the Tab. 3.

In general, the heatsink and the cooling systems (which define the thermal impedance Z_{h-a}) are designed to ensure that the steady-state junction temperature T_j of the semiconductor

Considering the environment temperature as T_a and the maximum heatsink temperature as $T_{h,max}$, the heatsink-to-environment thermal resistance can be approximated

Table 3 – Parameters of the thermal model.

Device	**Parameter**	**$Z_{j\text{-}c}$**				**$Z_{c\text{-}h}$**
IGBT	R_i $[K/W]$	0.0035	0.005	0.0069	0.010	0.024
	C_i $[J/K]$	0.5941	2.156	4.279	11.02	–
Diode	R_i [K/W]	0.0071	0.010	0.014	0.02	0.048
	C_i $[J/K]$	0.2933	1.063	2.104	5.727	–

by:

$$R_{h-a} = 6N\frac{T_{h,max} - T_a}{P_{lt}}, \tag{2.32}$$

where P_{lt} are the total power losses of the MMC in the worst operational case.

The power losses estimation is based on look-up tables, which is obtained from datasheets. Conduction losses, turn-on and turn-off energy for the IGBT's and the conduction and the reverse recovery energy for the diodes of each cell are considered (PEREIRA et al., 2016) Assuming that all the cell and arm parameters are identical, the losses and thermal behavior of all cells in the arms are similar. Hence, the loss evaluation can be simplified by consider only one arm of the converter.

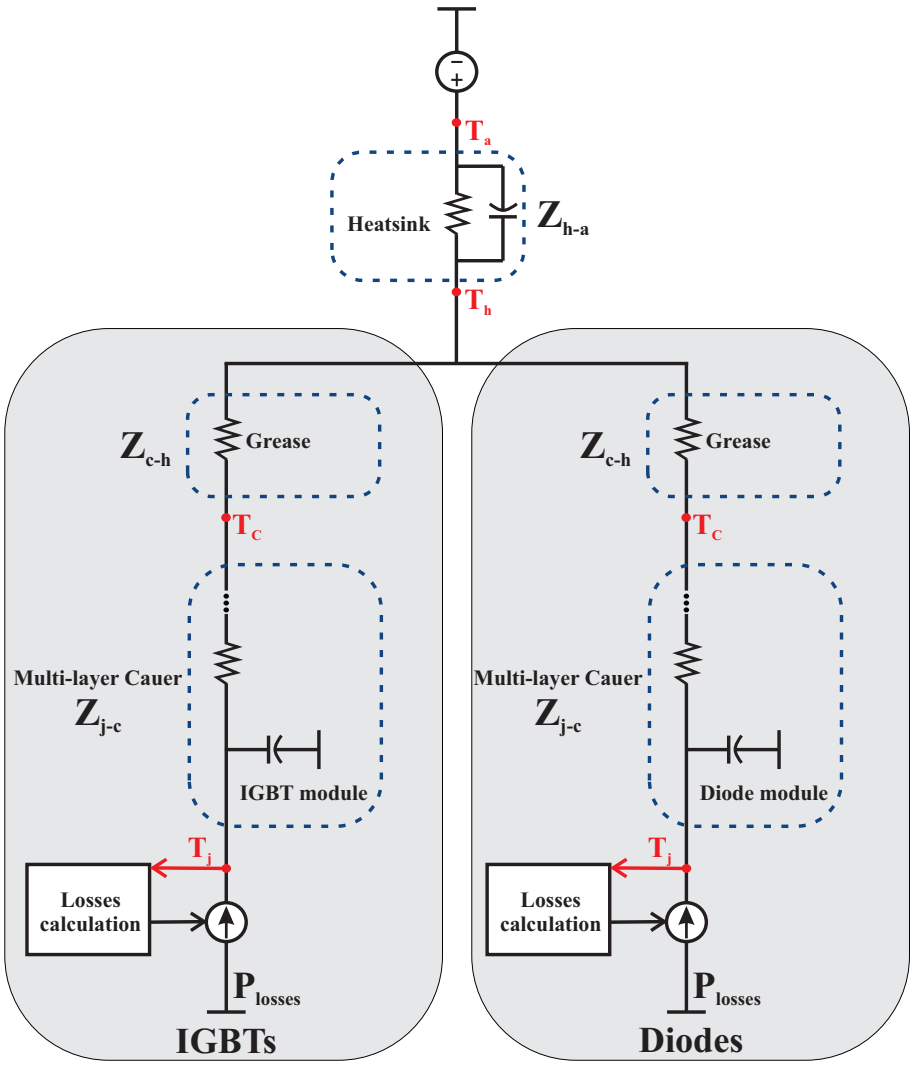

Figure 11 – Thermal model of the power devices with a common heatsink.

3 Methodology

This work is based on a 15 MVA STATCOM connected to 13.8 kV grid. The design of DSCC and DSBC-2L employs the methodology proposed in (CUPERTINO et al., 2017). In such conditions, the effective DC-link voltage is 25 kV. In order to use 3.3 kV semiconductor devices, 16 cells are necessary. Therefore, the voltage per cell is 1.56 kV. For the capacitor design, the energy storage is considered 40 kJ/MVA in order to guarantee 10 % of ripple at rated conditions, as suggested by (CUPERTINO et al., 2017).

For DSBC-3L, the DC-link voltage can be divided by two due to its ability to generate twice the voltage the DSCC and DSBC-2L, which is an advantage in terms of insulation. The capacitor voltages must be given by (2.12). Accordingly,

$$v'_{DC} = \frac{v_{DC}}{2}. \tag{3.1}$$

Therefore, in order to use the same semiconductor devices and the same cell voltage, the number of cells of DSBC-3L is given by:

$$v'^{*}_{cell} = v^{*}_{cell}, \tag{3.2}$$

$$\frac{1.5v'_{DC}}{N'} = \frac{v_{DC}}{N} \Leftrightarrow 1.5\frac{0.5v_{DC}}{N'} = \frac{v_{DC}}{N} \rightarrow N' = \frac{3}{4}N. \tag{3.3}$$

Therefore, the DSBC-3L presents 25 % less cells than DSCC and DSBC-2L. Regarding the capacitor design, the energy requirement is considered 24 kJ/MVA in order to guarantee 10 % of ripple at rated conditions. This value was obtained from (2.5), with $C = 4.1$ mF and $k_{dc} = 1.5$.

The parameters of the designed DSCC, DSBC-2L and DSBC-3L MMC STATCOM are presented in Tab. 4. The controller parameters are shown in Tab. 5. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method. These parameters were based in (CUPERTINO et al., 2017). The simulations were developed in the PLECS environment in order to validate the comparison between the topologies studied.

For this work, four case studies are presented in order to compare DSCC, DSBC-2L and DSBC-3L topologies:

- Case 1: Dynamic Simulation;
- Case 2: Current Distortion;

Table 4 – Parameters of the Modular Multilevel Converter

Parameters	**Topologies**	
	DSCC and DSBC-2L	***DSBC-3L***
Grid voltage (v_g)	13.8 kV	13.8 kV
Grid frequency (f_g)	60 Hz	60 Hz
Grid inductance (L_g)	1.3 mH	1.3 mH
Grid resistance (R_g)	0.0282 Ω	0.0282 Ω
DC-link voltage (v_{DC})	25 kV	12.5 kV
Rated power (S_n)	15 MVA	15 MVA
Arm inductance (L_{arm})	5.1 mH	5.1 mH
Arm resistance (R_{arm})	0.065 Ω	0.065 Ω
Cell capacitance (C)	5.12 mF	4.1 mF
Nominal cell voltage (v^*_{cell})	1.56 kV	1.56 kV
Carrier frequency (f_c)	270 Hz	270 Hz
Number of cells (N)	16	12

Table 5 – Parameters of the Controllers

Parameters	**DSCC and DSBC**
Sampling frequency	9720 Hz
Prop. gain of circulating current control	3.25
Resonant gain of circulating current control	1000
Circulating current LPF cut-off frequency	8 Hz
Prop. gain of individual balancing control	0.0004
Prop. gain of average control	9.7
Integ. gain of average control	165.5
Prop. gain of grid current control	8.09
Resonant gain of grid current control	1000
Moving average filter frequency	30 Hz

- Case 3: Power Losses;
- Case 4: Economic Evaluation.

3.1 Case 1: Dynamic Simulation

This case study considers three operational conditions, as illustrated in Fig. 12 and described bellow:

- $0 \leq t \leq$ 1s: -1 pu of reactive power is injected into the power grid (Capacitive Operation) and active power is zero;
- $1 < t \leq$ 1.5s: Reactive power increases at a rate of 4 pu/s until reaching 1 pu and active power is zero;

- $1.5 < t \leq 2.5$s: 1 pu of reactive power is injected into the power grid (Inductive Operation) and active power is zero.

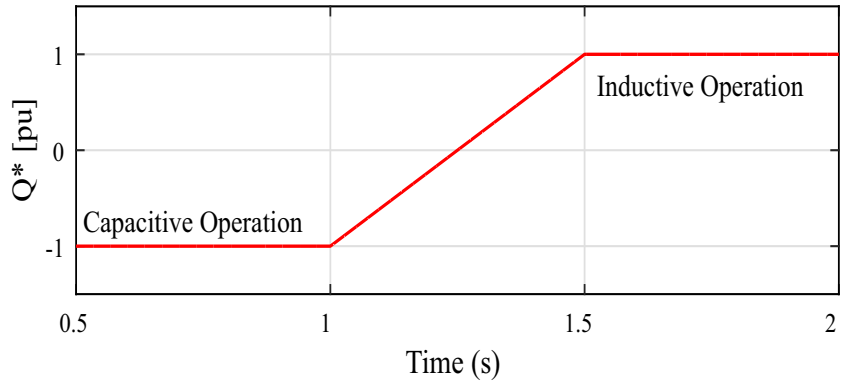

Figure 12 – Reactive power dynamic.

In order to compare the topologies, the capacitors voltage, the circulating current and the output power are analyzed.

3.2 Case 2: Current Distortion

In this case, a factor to be analyzed refers to Total Demand Distortion (TDD) of the output current, in order to verify the power quality. According to (IEEE. . . , 2014), the TDD analysis is made following the IEEE Std 519-2014 (Recommended Practice and Requirements for Harmonic Control in Electric Power Systems). In this recommendation, the TDD accounts the ratio of the root mean square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding inter harmonics, expressed as a percent of the maximum demand current. For this test, the injected reactive power is 1 *pu* capacitive and inductive.

3.3 Case 3: Power Losses

The conduction and switching losses in the semiconductors devices are evaluated. It was considered that the losses would be the same for each arm, so that the value of the total losses was the result of the value measured of the upper arm of phase A, for each of these variations, multiple by the number of arms. For this test, the injected reactive power is 1 *pu* capacitive and inductive.

Therefore, considering $T_a = 40°C$, $T_{h,max} = 70°C$ in the worst case and P_{lt} as 0.5 % of rated power, the following thermal resistances are obtained from (2.32):

Table 6 – Thermal resistances.

Topologies	Thermal Resistance
DSCC	0.0384 k/W
DSBC-2L	0.0384 k/W
DSBC-3L	0.0288 k/W

3.4 Case 4: Economic Evaluation

Regarding the economic evaluation, the costs in relation to the capacitors and the semiconductors devices are analyzed.

Thus, in order to evaluate the economic costs in relation to the capacitors of the cells, the total energy stored is calculated. The minimum value of the nominal energy storage per arm, is given by:

$$E_{nom} = \frac{CNv_{cell}^2}{2}. \tag{3.4}$$

The total energy storage in the MMC is $6E_{nom}$. The cost of the capacitors of the converters is approximated from the current market prices and is considered as 150 e/kJ, according to (ENGEL et al., 2015).

The cost of the semiconductor devices, controls, cabinets, among others of the converters is approximated from the current market prices and it is considered as 3.5 e/kVA, of the installed switching power P_{switch}, which is defined as (ENGEL et al., 2015; SIDDIQUE et al., 2016):

$$P_{switch} = N_{semi}U_{block}I_{nom}. \tag{3.5}$$

4 Results and Discussion

4.1 Case 1: Dynamic Simulation

Fig. 13 illustrates the capacitors voltage for the topologies presented. For both the ripple is presented in detail for capacitive and inductive operation. In both topologies, the voltage ripple of the capacitors remained within the limit of 10 % of capacitance tolerance. For the capacitive and inductive operations, the average voltage is represented by AVG. This average value is considered in the calculation of the total energy stored in (CUPERTINO et al., 2017). In addition, this value must be within the established tolerance limits of ±10 % of v^*_{cell}.

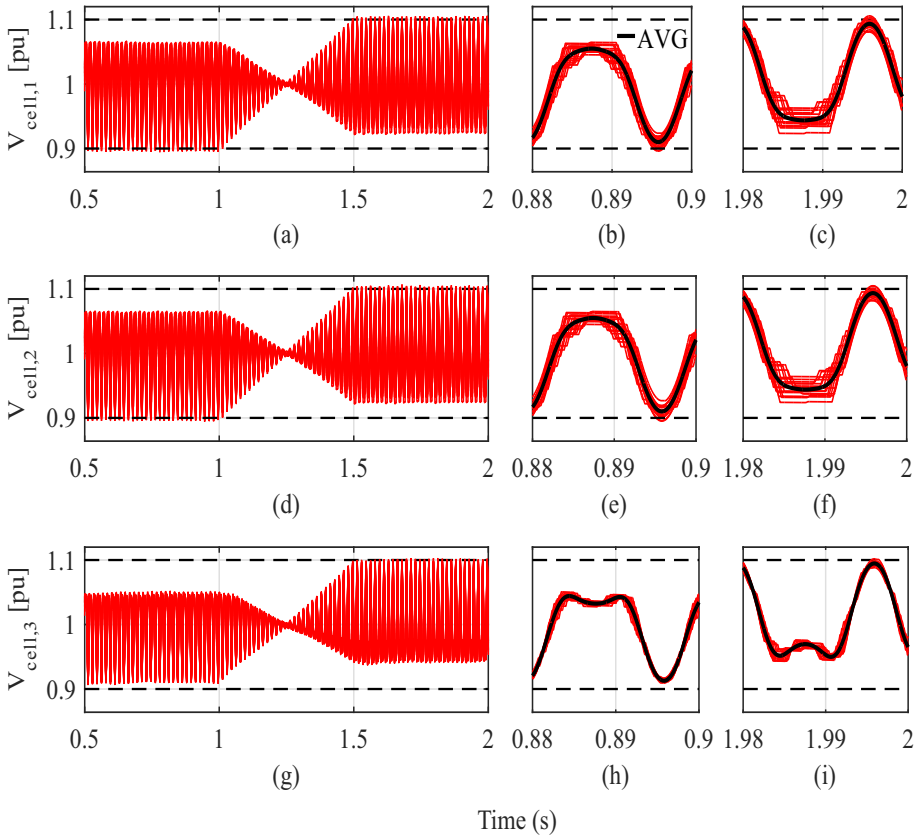

Figure 13 – Capacitors Voltage: (a) DSCC; (b) detail in capacitive operation of DSCC; (c) detail in inductive operation of DSCC; (d) DSBC-2L; (e) detail in capacitive operation of DSBC-2L; (f) detail in inductive operation of DSBC-2L; (g) DSBC-3L; (h) detail in capacitive operation of DSBC-3L; (i) detail in inductive operation of DSBC-3L.

The dynamic response and the difference among the maximum and minimum peak of the circulating current can be observed in Fig. 14. As noted, DSBC-3L presents a higher

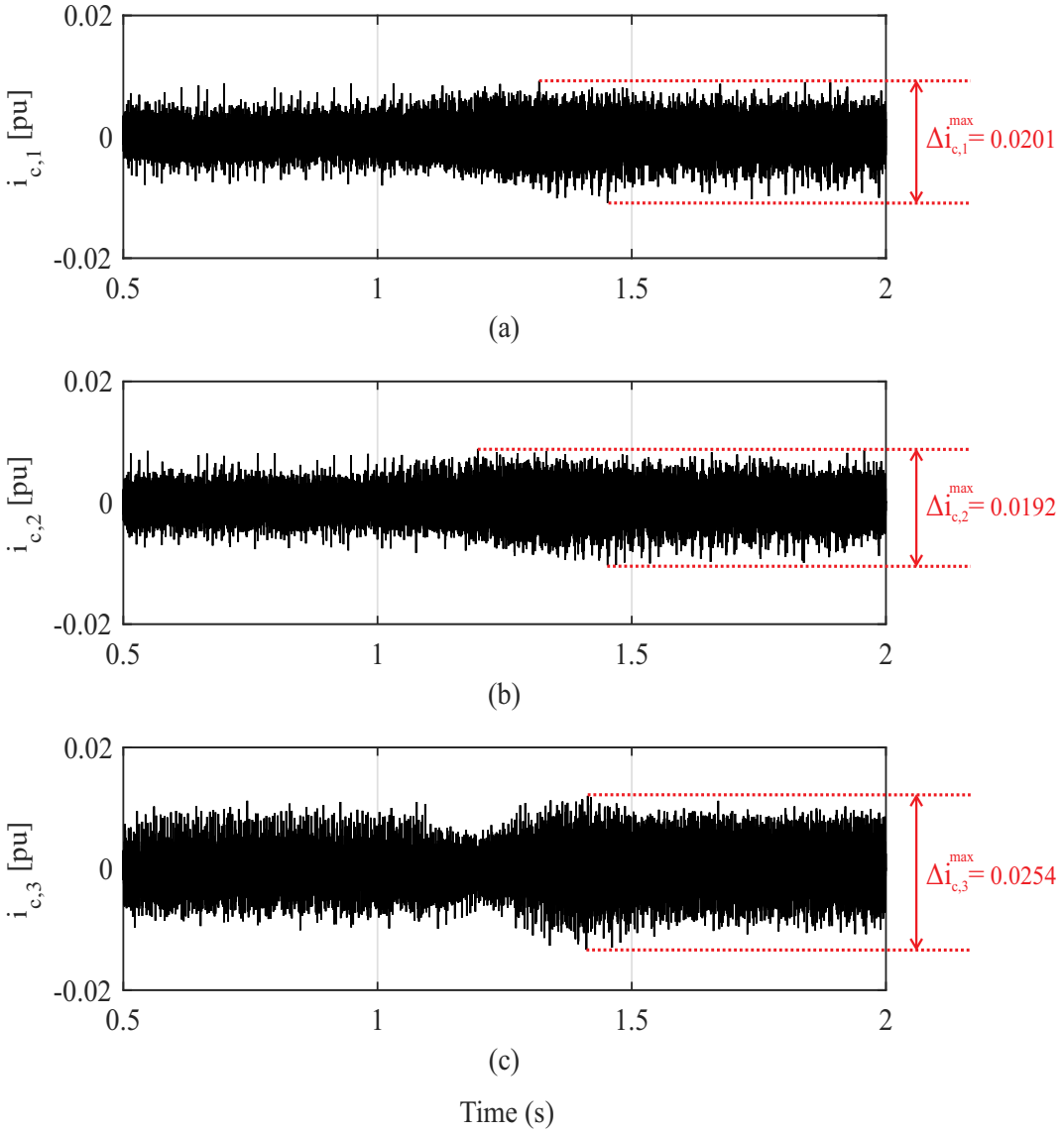

Figure 14 – Circulating current: (a) DSCC; (b) DSBC-2L; (c) DSBC-3L.

ripple in the capacitive and inductive operations, being 1.26 times larger than DSCC and 1.32 times larger than DSBC-2L. This is due to the reduction of the number of cells.

The active and reactive power of the grid is shown in Fig. 15. For the topologies presented, the oscillation in the power response is smaller than 5.2 %. However, due to the decrease of the number of cells in the DSBC-3L, this topology presents greater oscillation than the other two topologies. Indeed, as shown in Fig. 16 and Fig. 17, the DCBC-3L has the highest value of reactive power absolute error in relation to the reference capacitive and inductive operations, which 0.0393 pu and 0.0515 pu, respectively.

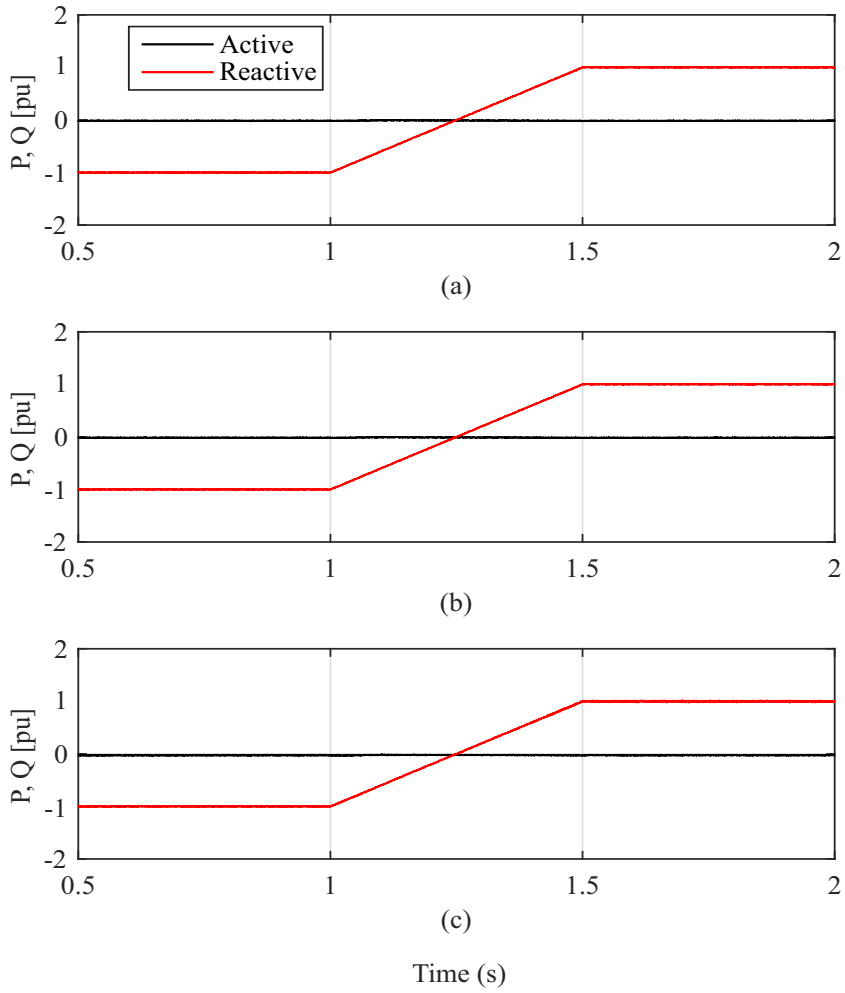

Figure 15 – Output power measured: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

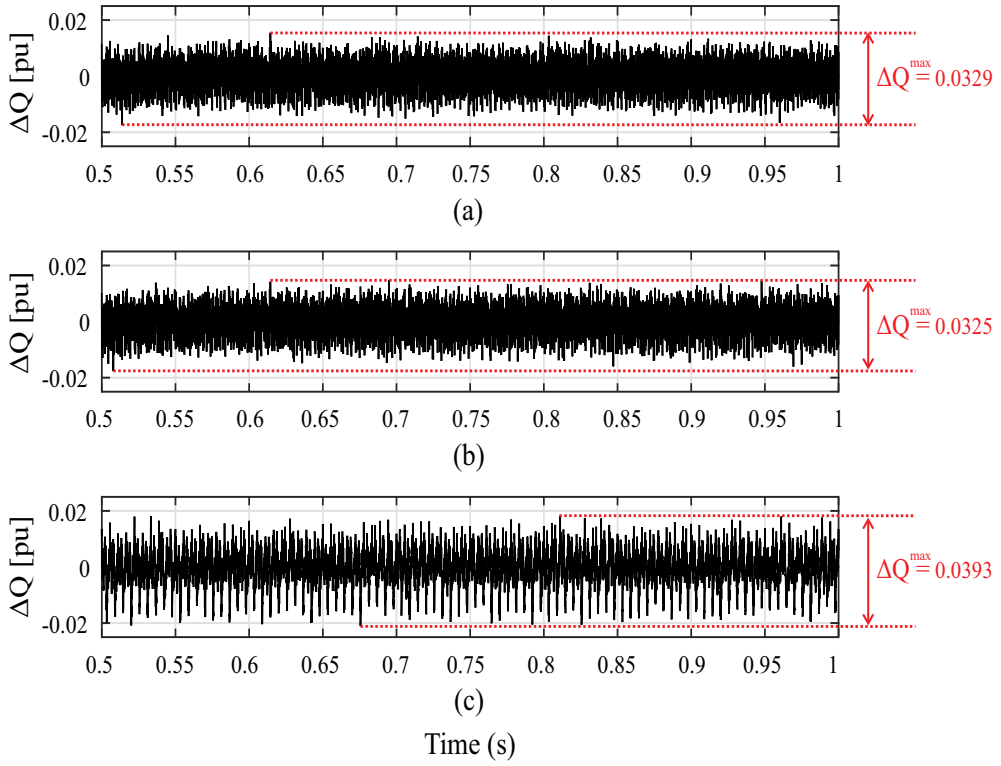

Figure 16 – Reactive power absolute error in the capacitive operation: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

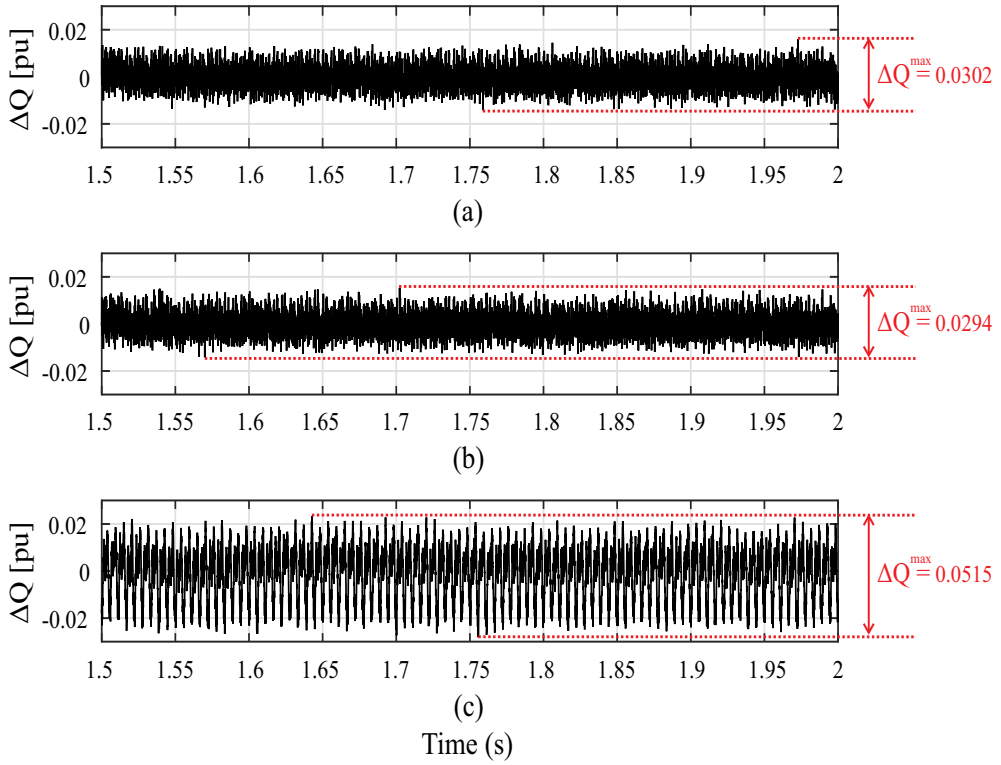

Figure 17 – Reactive power absolute error in the inductive operation: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

4.2 Case 2: Current Distortion

In order to evaluate the quality of the output current the TDD is evaluated, as can be seen in Fig. 18. For DSBC-3L the value is higher than the other topologies, which presented similar values. The TDD value of the DSBC-3L can be explained by the increase of the circulating current while compared of the others topologies due to the decrease of the number of cells. However, the topologies fall into the recommendation proposed in (IEEE. . . , 2014) to a maximum of 5 %.

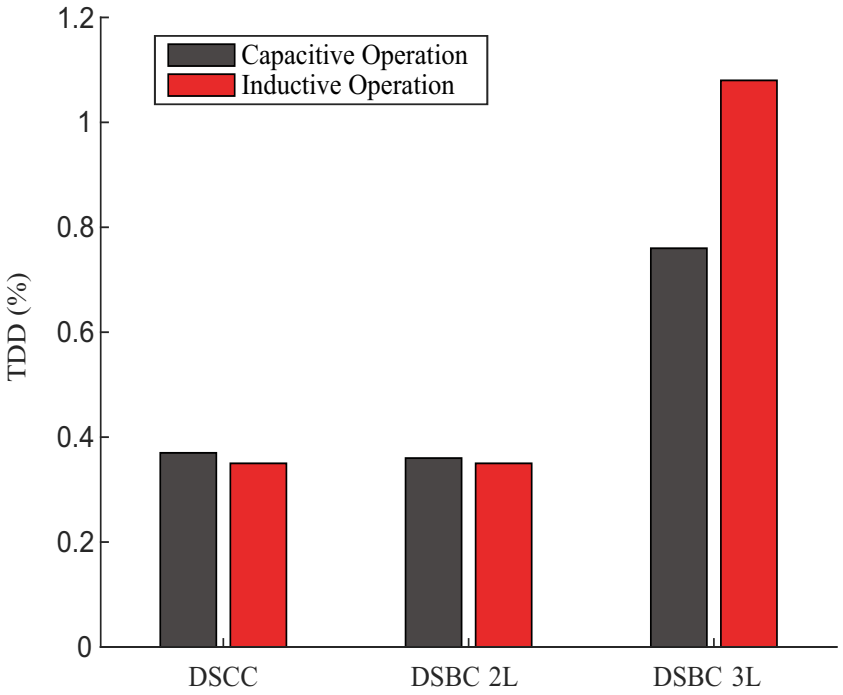

Figure 18 – Total Demand Distortion of Output Current.

4.3 Case 3: Power Losses

The power losses of the MMC are also evaluated, as shown in Fig. 19. The analyzed MMC topologies are performed from the calculation of conduction and switching losses for one arm of the converter on semiconductors devices. In relation to capacitive and inductive operation, the values of power losses are similar. When analyzed in relation to the topologies, the DSBC-2L presents almost twice higher power losses. Indeed, the DSBC-2L has higher number of semiconductors when compared to the DSCC topology. The DSBC-3L shows power losses between those presented in the other two topologies.

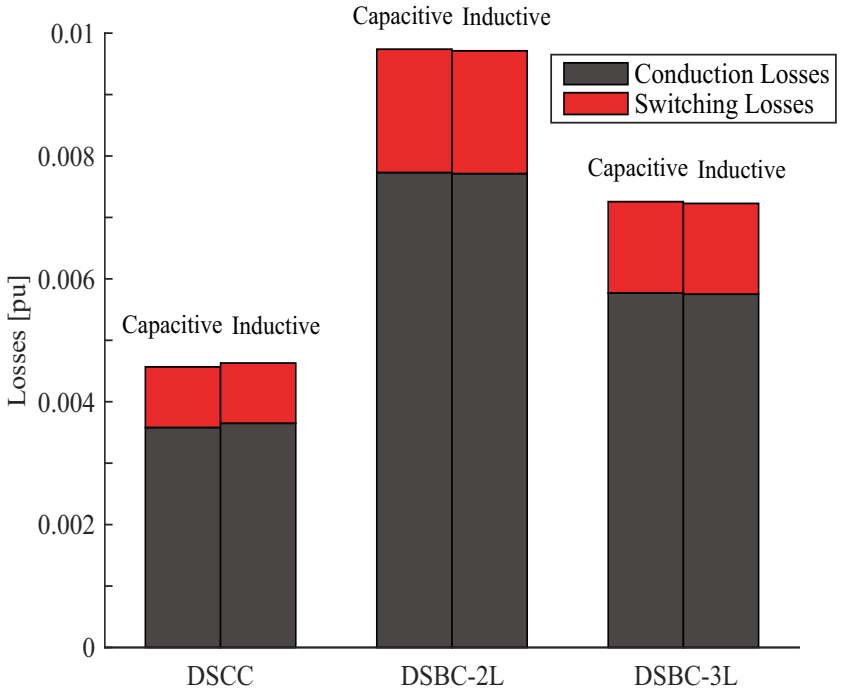

Figure 19 – Power losses.

4.4 Case 4: Economic Evaluation

Finally, the cost is evaluated and the total energy storage and the installed switching power is shown in Tab. 7 and the cost of both in Tab. 8. From these values, the total economic evaluation is presented in Tab. 9. Considering the cost for kJ, it is possible to verify that the cost in relation to the capacitors is the same for the DSCC and DSBC-2L because the total stored energy in the converter is the same. In the DSBC-3L the total stored energy required is small, resulting in lower costs. Regarding the costs of semiconductors, the DSBC-2L presents a higher value when compared to the other two cases due to the greater number of semiconductor devices in its design. The DSBC-3L shows costs of semiconductors between those presented in the other two topologies. DSCC presented the smaller costs (1 pu) in relation of the DSBC-2L, that presented the highest cost (1.96 pu).

Table 7 – Total Energy Storage and Installed Switching Power

Topologies	**Total Energy Storage**	$\mathbf{P_{switch}}$
DSCC	600 kJ	576 MVA
DSBC-2L	600 kJ	1152 MVA
DSBC-3L	360.2 kJ	864 MVA

Because the pole-to-pole voltage of the DSBC-3L is half the bus value of the DSCC and DSBC-2L, the insulation costs are lower. However, this work does not include in the cost analysis in relation to this requirement.

Table 8 – Costs of Total Energy Storage and Installed Switching Power

Topologies	**Total Energy Storage**	$\mathbf{P_{switch}}$
DSCC	1 pu	1 pu
DSBC-2L	1 pu	2 pu
DSBC-3L	0.6 pu	1.5 pu

Table 9 – Economic Evaluation

Topologies	**Investment Costs**
DSCC	1 pu
DSBC-2L	1.96 pu
DSBC-3L	1.46 pu

4.5 Summary of Results

Based on the results presented, Tab. 10 summarizes the requirements considered important for comparison of the topologies studied, where "++" denotes good characteristics, "+" denotes acceptable characteristics and "-" denotes poor characteristics.

Table 10 – Requirements of the topologies

Requirements	**DSCC**	**DSBC-2L**	**DSBC-3L**
Number of Semicon. Devices	++	-	+
Power Losses	++	-	+
Number of Cells	+	+	++
Economic Costs of Capacitors	+	+	++
Economic Costs of Semicon. Devices	++	-	+
Economic Costs of Insulation Bus	+	+	++
Capacity of DC Fault Blocking	-	++	++

The insulation bus and capacity of DC fault blocking were not addressed in this study. Thus, only the STATCOM operation was studied.

5 Conclusion

In this work, the topologies (DSCC, DSBC-2L and DSBC-3L) are compared in terms of operational characteristics for a STATCOM system, considering a 15 MVA MMC connect to a 13.8 kV grid. The main circuit parameters, such as capacitor voltages, circulating current, mains current distortion, active and reactive power delivered and converter implementation costs were studied. The implemented control strategies are validated together with the modulation strategies applied in the study topologies, DSBC and DSCC, a fact evidenced mainly by the synthesized output voltages and harmonic distortion analysis of the grid current.

Based on the operating characteristics, costs and losses, associated with the steady-state operation of the MMC was verified. The circulating current shown a small ripple for the both topologies presenting a slightly larger ripple on the DSBC-3L. In terms of current distortion, there is more harmonic distortion in the output current for the DSBC-3L, when compared to the others, however the topologies has TDD according to IEEE Std 519-2014. In terms of losses, the DSCC presented the lowest losses and the DSBC-2L presented the highest losses. The DSBC-3L has intermediate characteristics when compared to the other two topologies. Also, for the cost analysis, the same logic is observed.

Therefore, this work validated that the structure DSBC-3L is between the topologies DSCC and DSBC-2L in terms of costs, dynamics and losses. The DSBC-3L presents advantageous in terms of protection against failures for HVDC transmission systems with STATCOM operation during pole-to-pole DC short-circuits, for example, due to its Bridge-Cell structure. In addition, it presents a reduction of the insulation costs, due to the use of a smaller bus. These two characteristics were not addressed in this study because the STATCOM operation was studied. When the DSBC-2L and DSBC-3L topologies were compared, the latter proved to be promising under the presented application conditions, which reveals its importance in studies and future applications in physical systems.

6 Continuity Proposals

As a proposal for continuity of this work, the following points are cited for a better comparison of the presented topologies.:

- Energy requirement analysis for DSBC-3L topology;
- Thermal stress analysis of the semiconductors devices;
- Lifetime evaluation including semiconductor power devices and capacitors;
- Analyze the impact of using another modulation strategy such as Nearest Level Control (NLC);
- Analyze the impact of using another types of cell;
- Analyse the impact of Unipolar, Bipolar and Hybrid techniques PWM Modulation for DSBC topology;
- Analysis of the voltage synthesized by Chopper and Bridge cells with open circuit failure in the IGBTs;
- Analysis of the behavior of the DS topologies in a DC-link short-circuit for HVDC transmission systems with STATCOM operation during pole-to-pole DC short-circuits, due to DSBC capacity of DC fault blocking.

References

AKAGI, H. Classification, terminology, and application of the modular multilevel cascade converter (mmcc). *IEEE Transactions on Power Electronics*, v. 26, n. 11, p. 3119–3130, Nov 2011. ISSN 0885-8993. 18, 19, 20

AKAGI, H.; WATANABE, E. H.; AREDES, M. The instantaneous power theory. In: _____. *Instantaneous Power Theory and Applications to Power Conditioning*. [S.l.]: IEEE, 2007. 26

ALLU, A.; ODAVIC, M.; ATALLAH, K. Design considerations of a full bridge modular multilevel converter under variable dc link voltage. In: *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. [S.l.: s.n.], 2017. p. 504–510. 19

CAMARGO, R. S. et al. Design and analysis methodology for modular multilevel converters (mmc). *IEEE Latin America Transactions*, v. 16, n. 4, p. 1105–1112, April 2018. ISSN 1548-0992. 18

CUPERTINO, A. et al. Dscc-mmc statcom main circuit parameters design considering positive and negative sequence compensation. v. 29, 11 2017. 18, 21, 22, 23, 24, 27, 29, 33, 36, 40

DHAL, P. K.; RAJAN, C. C. A. Design and analysis of statcom for reactive power compensation and transient stability improvement using intelligent controller. In: *2014 International Conference on Electronics and Communication Systems (ICECS)*. [S.l.: s.n.], 2014. p. 1–6. 17, 21

ENGEL, S. P. et al. Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids. *IEEE Transactions on Power Electronics*, v. 30, n. 1, p. 124–137, Jan 2015. ISSN 0885-8993. 39

FARIAS, J. V. M. et al. On the redundancy strategies of modular multilevel converters. *IEEE Transactions on Power Delivery*, v. 33, n. 2, p. 851–860, April 2018. ISSN 0885-8977. 18

FUJII, K.; SCHWARZER, U.; DONCKER, R. W. D. Comparison of hard-switched multi-level inverter topologies for statcom by loss-implemented simulation and cost estimation. In: *2005 IEEE 36th Power Electronics Specialists Conference*. [S.l.: s.n.], 2005. p. 340–346. ISSN 0275-9306. 21, 22, 25

HAGIWARA, M.; AKAGI, H. Control and experiment of pulsewidth-modulated modular multilevel converters. *IEEE Transactions on Power Electronics*, v. 24, n. 7, p. 1737–1746, July 2009. ISSN 0885-8993. 18, 19, 27

HE, L. et al. Low-frequency ripple suppression for medium-voltage drives using modular multilevel converter with full-bridge submodules. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 4, n. 2, p. 657–667, June 2016. ISSN 2168-6777. 19, 25

IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems. *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, p. 1–29, June 2014. 38, 44

ILVES, K. et al. Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters. *IEEE Transactions on Power Electronics*, v. 27, n. 1, p. 57–68, Jan 2012. ISSN 0885-8993. 24

ILVES, K. et al. Analysis and operation of modular multilevel converters with phase-shifted carrier pwm. *IEEE Transactions on Power Electronics*, v. 30, n. 1, p. 268–283, Jan 2015. ISSN 0885-8993. 18, 24, 29

ILVES, K. et al. On energy storage requirements in modular multilevel converters. *IEEE Transactions on Power Electronics*, v. 29, n. 1, p. 77–88, Jan 2014. ISSN 0885-8993. 23

KAWAMURA, W.; HAGIWARA, M.; AKAGI, H. Control and experiment of a modular multilevel cascade converter based on triple-star bridge cells. *IEEE Transactions on Industry Applications*, v. 50, n. 5, p. 3536–3548, Sept 2014. ISSN 0093-9994. 19

KONTOS, E. et al. High order voltage and current harmonic mitigation using the modular multilevel converter statcom. *IEEE Access*, v. 5, p. 16684–16692, 2017. ISSN 2169-3536. 17, 18

LAMB, J.; MIRAFZAL, B.; BLAABJERG, F. Pwm common mode reference generation for maximizing the linear modulation region of chb converters in islanded microgrids. *IEEE Transactions on Industrial Electronics*, v. 65, n. 7, p. 5250–5259, July 2018. ISSN 0278-0046. 29

LI, B. et al. Analysis of the phase-shifted carrier modulation for modular multilevel converters. *IEEE Transactions on Power Electronics*, v. 30, n. 1, p. 297–310, Jan 2015. ISSN 0885-8993. 19

MA, Y.; HUANG, A.; ZHOU, X. A review of statcom on the electric power system. In: *2015 IEEE International Conference on Mechatronics and Automation (ICMA)*. [S.l.: s.n.], 2015. p. 162–167. ISSN 2152-7431. 17

MARQUARDT, R. Stromrichterschaltungen mit verteilten energiespeichern. *German Patent DE20 122 923 U1*, 2001. 18

MORA, A. et al. Dead-time and semiconductor voltage drop compensation for cascaded h-bridge converters. *IEEE Transactions on Industrial Electronics*, v. 63, n. 12, p. 7833–7842, Dec 2016. ISSN 0278-0046. 29

PADIYAR, K. R. *FACTS Controllers in Power Transmission and Distribution*. New Delhi: New Age International Publishers, 2007. 549 p. 17

PEREIRA, H. A. et al. Capacitor voltage balance performance comparison of mmc-statcom using nlc and ps-pwm strategies during negative sequence current injection. In: *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*. [S.l.: s.n.], 2016. p. 1–9. 33, 34

PEREIRA, M. et al. Svc plus: An mmc statcom for network and grid access applications. In: *2011 IEEE Trondheim PowerTech*. [S.l.: s.n.], 2011. p. 1–5. 17

PEREZ, M. A. et al. Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. *IEEE Transactions on Power Electronics*, v. 30, n. 1, p. 4–17, Jan 2015. ISSN 0885-8993. 18

SHINDE, O. K.; PULAVARTHI, V. R. S. V. B. Statcom converters and control: A review. In: *2017 International Conference on Data Management, Analytics and Innovation (ICDMAI)*. [S.l.: s.n.], 2017. p. 145–151. 17

SIDDIQUE, H. A. B. et al. Comparison of modular multilevel and neutral-point-clamped converters for medium-voltage grid-connected applications. In: *2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA)*. [S.l.: s.n.], 2016. p. 297–304. 39

SINGH, B. et al. Static synchronous compensators (statcom): a review. *IET Power Electronics*, v. 2, n. 4, p. 297–324, July 2009. ISSN 1755-4535. 17

THITICHAIWORAKORN, N.; HAGIWARA, M.; AKAGI, H. Experimental verification of a modular multilevel cascade inverter based on double-star bridge-cells (mmci-dsbc). In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. [S.l.: s.n.], 2012. p. 4196–4202. ISSN 2329-3721. 27

TU, Q. et al. Parameter design principle of the arm inductor in modular multilevel converter based hvdc. In: *2010 International Conference on Power System Technology*. [S.l.: s.n.], 2010. p. 1–6. 24

XIA, Y.; AYYANAR, R. Comprehensive comparison of thd and common mode leakage current of bipolar, unipolar and hybrid modulation schemes for single phase grid connected full bridge inverters. In: *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*. [S.l.: s.n.], 2017. p. 743–750. ISSN 2470-6647. 31

ZHANG, J.; ZHAO, C. The research of sm topology with dc fault tolerance in mmc-hvdc. *IEEE Transactions on Power Delivery*, v. 30, n. 3, p. 1561–1568, June 2015. ISSN 0885-8977. 19

ZHAO, C. et al. Energy storage requirements of full-bridge modular multilevel converter with zero sequence voltage injection. In: *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*. [S.l.: s.n.], 2017. p. 4512–4517. 19

ZHAO, C. et al. Optimized design of full-bridge modular multilevel converter with low energy storage requirements for hvdc transmission system. *IEEE Transactions on Power Electronics*, v. 33, n. 1, p. 97–109, Jan 2018. ISSN 0885-8993. 19