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Comparison of Double Star Topologies of Modular Multilevel Converters in STATCOM Application

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***Abstract*—The modular multilevel converters (MMCs) have shown great emphasis in academic studies of the last decades, specially applied in renewable energy systems, HVDC systems, energy storage, electrical drives and STATCOMs. In STATCOM applications, in particular, the Double Star (DS) configuration has several operating advantages, mainly related to its ability to compensate negative sequence components and unbalanced currents. Considering the advantage of these topologies in STATCOM application, it is proposed in this work a comparison of two DS topologies: Double Star Chopper-Cell (DSCC) and Double Star Bridge-Cell (DSBC). These topologies are compared in terms of steady-state operation, power losses and costs. In addition, two variations of DSBC topology are approached: DSBC-2L, which employs 2-level modulation and DSBC-3L, which employs 3-level modulation. The three MMC topologies are designed based on a 15 MVA STATCOM connected in a 13.8 kV grid. The simulation results validate the design methodology and also indicates the DSBC-3L topology as a promising solution for medium voltage STATCOMs due to its costs, protection during short circuits and smaller insulation requirements.**

***Index Terms*—Modular Multilevel Converter, STATCOM, Double Star Topologies, DSCC, DSBC-2L, DSBC-3L, Modulation Strategies.**

I. Introduction

The process of generation, transmission and distribution of energy is characterized by complex problems of integration and operation [1]. In recent years, a large increase in the types of loads connected to the grid, and especially those of non-linear characteristics, such as electric drives, and electric arc furnace, have increased in medium voltage systems [2].

Due to this fact, the distribution grid suffer with these load impacts in the grid voltage regulation. As a solution to this problem there is the static synchronous compensator (STATCOM) [1]–[3], which can compensate positive and negative sequence reactive power and low frequency active power component.

Additionally, in the last decades, the use of high power equipments applied especially in industrial plants and large consumers, have been increasing and making operation with higher voltage levels necessary. Thus, the use of conventional converters become unfeasible, in particular, related to the physical limitation of the semiconductor blocking voltage capability [4]. Due to these challenges, studies were proposed with alternative topologies, such as Modular Multilevel Converter (MMC) [5]. This converter has superior characteristics when compared to the others topologies, such as: modularity, high efficiency, low harmonic content, redundancy, high reliability and others [4], [6].

Moreover, the MMC presents several construction topologies for three-phase or single phase systems. The MMC topologies differ in relation to the type of connection and also to the type of cell. This paper has as main focus to compare different types of cells. These MMC cells can be classified according to the capacity of voltage synthesis. In traditional applications, the cells can present two or three output levels, such as the chopper-cell (CC) or the bridge-cell (BC), respectively [7].

The capacity to synthesize voltage levels across the cell is linked to the capacitor voltage (V_c). While for the CC, the synthesis levels are restricted between 0 and $+V_c$, the BC additionally synthesizes $-V_c$ [8]. In most of the academic works, the use of the BC is proposed due to the protection and voltage synthesis characteristics. However, some studies operate with the BC at two voltage levels (0 and V_c), as in [9]. On the other hand, others work with the BC operating with three voltage levels ($-V_c$, 0 and V_c), as in [10].

Reference [6] proposes the following classification and terminology of the MMC family:

- Single-Star Bridge-Cells MMC (SSBC);
- Single-Delta Bridge-Cells MMC (SDBC);
- Double-Star Chopper-Cells MMC (DSCC);
- Double-Star Bridge-Cells MMC (DSBC);

Among these topologies, the DSCC and DSBC are the most applied in transmission systems. The operating characteristics of the DSBC are superior in terms of the voltage synthesis capability at the converter output, as well as protection capability in case of a dc-link short-circuit. Additionally, DSBC topology presents more degrees of freedom in terms of modulation. Then, the 2-level and 3-level modulation

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can be used. These two variations of DSBC topology are called in this paper of DSBC-2L and DSBC-3L, respectively [8], [11]. On the other hand, the DSCC topology has the advantage of reduced power losses due to the smaller number of semiconductors when compared with DSBC.

In this context, this paper aims to make the comparison between three different MMC topologies, DSCC, DSBC-2L and DSBC-3L, working as STATCOM applied in a three phase system. The modulation strategies for each topology are presented, as well as the switching strategy. In this way, the contributions of this work can be summarized as:

- Compare the operational characteristics of Double-Star MMC topologies;
- Carry out a study of cost and power losses between the studied topologies;
- Evaluate the control strategies for chopper-cell and bridge-cell structures in Double Star topologies;
- Evaluate the advantages and disadvantages of the DS MMC topologies;

This work is outlined as follows. Section II presents the MMC topologies: DSCC, DSBC-2L and DSBC-3L. Section III presents the control design. Section IV discusses the modulation strategies. Section V shows the case study and the parameters of the simulated model. The obtained results are discussed in Section VI. Finally, the conclusion of this work are stated in section VII.

II. MMC Topologies

Fig. 1 shows the MMC STATCOM topologies employed in this work, with N cells per arm. Each MMC cells contain a capacitor C, and four or eight semiconductor switches, depending of the types cells (CC or BC). The first, DSCC, is composed by four semiconductors, illustrated in Fig. 1(b). The second, DSBC, is composed by eight semiconductors, illustrated in Fig. 1(c).

The L_{arm} is responsible to reduce the harmonics in the circulating current and also limiting the currents during possible faults. The arm resistance R_{arm} represents the intrinsic resistance of arm inductance. However, it is not illustrated. Usually, in parallel with each cell, there is a switch S_T, which bypasses the cell in case of failures. The choice of this topology can be justified in terms of flexibility, because it is possible to control negative-sequence reactive power and consequently control the circulating current among the three legs of the Double Star topology [1].

III. Control Strategy

The control strategy for the Double-Star MMC STATCOM is shown in Fig. 2 [12]. The Fig. 2 presents the grid current control, the circulating current control and the individual balancing control. The control strategy of the grid current control is carried out through the derivation of components in stationary ($\alpha\beta$) reference frame, which results in the simultaneous control of negative and positive sequence of the grid current and voltage. The control generates an output for each phase. The total number of cells is 6N, due to the presence of 6 arms in the three-phase system.

The outer loop controls the square of the average voltage v_{avg} of all cells of the converter. This average voltage is defined by:

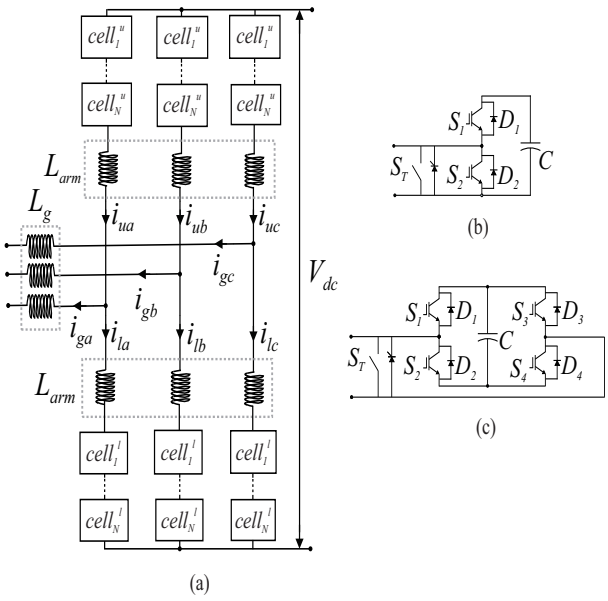

Fig. 1. (a) Schematic of the Double-Star MMC; (b) Chopper-Cell; (c) Bridge-Cell.

$$v_{avg} = \frac{1}{6N}\sum_{i=1}^{6N} v_{cell,i}, \tag{1}$$

where $v_{cell,i}$ is the *i*-th cell voltage.

The average voltage reference v^*_{avg} and v^*_{cell} of the DSCC and the DSBC-2L are expressed by:

$$v^*_{avg} = v^*_{cell} = \frac{V_{dc}}{N}, \tag{2}$$

where V_{dc} is the nominal pole to pole dc voltage. Although there is no connection on the dc-link in the DSCC-MMC STATCOM, this value is an important parameter to avoid over-modulation [13].

Nevertheless, according to [9], in order to guarantee correct operation, the capacitor voltages of the DSBC-3L must be given by:

$$v'^*_{avg} = v'^*_{cell} = \frac{1.5V'_{dc}}{N'}, \tag{3}$$

where the subscript $'$ indicates variables for DSBC-3L.

The reference calculator in Fig. 2 is used to compute the active power P^* that flows to the converter. Using the instantaneous power theory [14], it is possible to express the grid current by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = v_{g\alpha\beta} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} + \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix}, \tag{4}$$

where $v_{g\alpha\beta}$ is defined by:

$$v_{g\alpha\beta} = \frac{1}{v^2_{g\alpha} + v^2_{g\beta}}. \tag{5}$$

The circulating current control, presented in Fig. 2, is responsible for reducing the harmonics in the circulating current and inserting damping in the converter dynamic

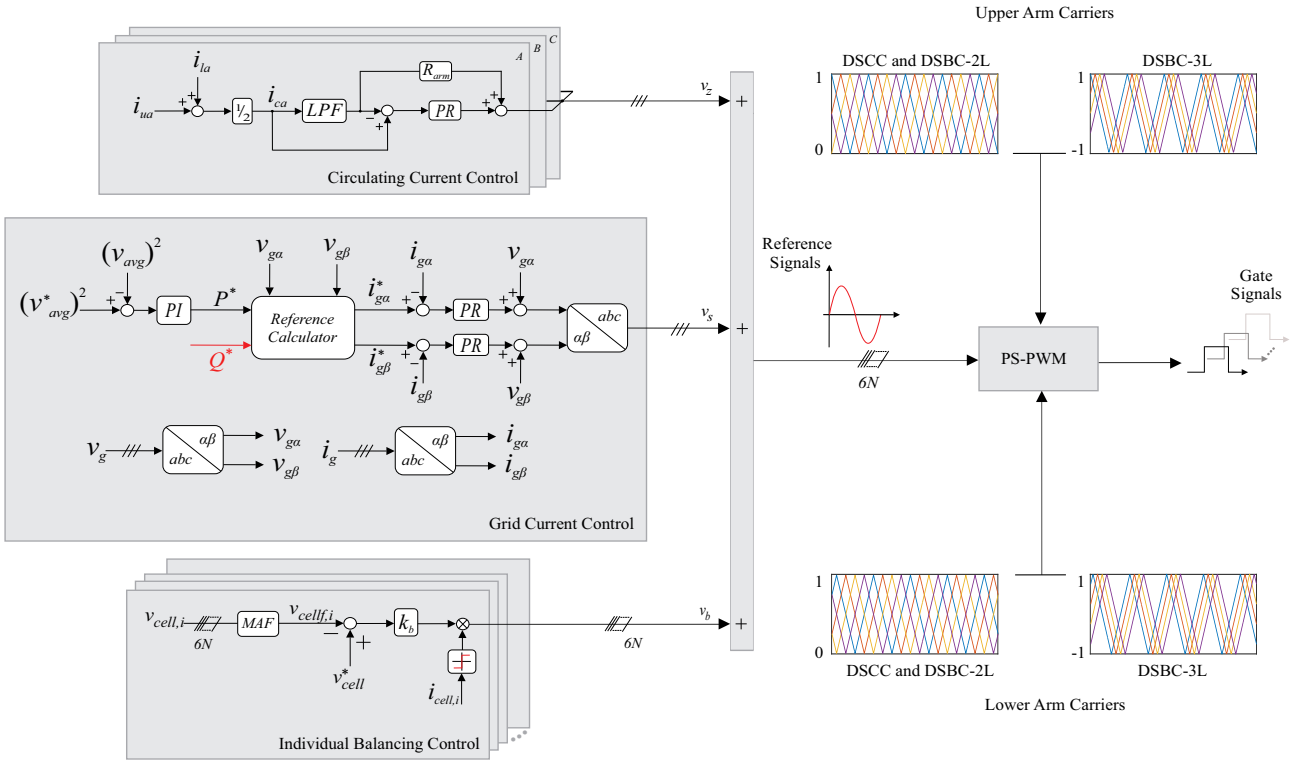

Fig. 2. Control strategy for MMC-STATCOM: circulating current, grid current and individual balancing control.

response. The circulating current is calculated per converter leg and is given by:

$$i_c = \frac{i_u + i_l}{2}. \tag{6}$$

Regarding to the modulation strategy, it is apply the Phase-Shifted Pulse Width Modulation (PS-PWM). For PS-PWM method, an extra individual balancing control loop, presented in Fig. 2, is necessary to maintain the capacitor voltages following the reference $v^*_{cell,j}$ in the individual balancing control [10].

The reference signals depends on the output signals, shown in Fig. 2. The normalized references to the DSCC and DSBC topologies are obtained given by [15], and expressed to:

$$v_{u,n} = v_b + \frac{v_z}{v^*_{cell}} - \frac{v_s}{N v^*_{cell}} + \frac{1}{2}, \tag{7}$$

$$v_{l,n} = v_b + \frac{v_z}{v^*_{cell}} + \frac{v_s}{N v^*_{cell}} + \frac{1}{2}. \tag{8}$$

For the voltage reference (v_s), the injection of 1/6 of third harmonic is used in order to increase the linear operational area of the modulation curve [15].

IV. Modulation Strategies

Among the modulation strategies typically employed in MMC, this work considers the PS-PWM [10]. The angular displacements of the carrier waveforms can be chosen in terms of the desired harmonic performance. The angle expressed in (9), for DSCC and DSBC-2L, shows the existing lag in the upper and lower arm carriers, in turn the β, angle indicates the angular displacement between the carrier waveforms in the upper and lower arms.

$$\theta_{u,n} = \pi(\frac{n-1}{N}) \text{ and } \theta_{l,n} = \theta_{u,n} + \beta, \tag{9}$$

where n = 1,2,..,N.

According to [12], two different modulation strategies can be employed: (N + 1) level modulation, with $\beta = \pi$ and (2N + 1) level modulation, with β being presented by (10) and (11). In STATCOM applications, the ac side power quality is taken with priority. In this way the modulation level (2N + 1) is employed in the PS-PWM strategy [12], [15].

$$\beta = \frac{\pi}{N}, \text{ if N is even,} \tag{10}$$

and

$$\beta = 0, \text{ if N is odd.} \tag{11}$$

For the topology DSBC-3L the angular displacements can be expressed by [16], [17]:

$$\theta'_{u,n} = \pi(\frac{n-1}{2N}) \text{ and } \theta'_{l,n} = \theta'_{u,n} + \beta', \tag{12}$$

where n = 1,2,..,N and β' is defined as:

$$\beta' = \frac{\pi}{2N}, \text{ if N is even,} \tag{13}$$

and

$$\beta' = 0, \text{ if N is odd.} \tag{14}$$

TABLE I
SWITCHING STATES OF THE CHOPPER-CELL SWITCHES

State	S_1	S_2	V_{cell}
1	1	0	$+V_c$
2	0	1	0

TABLE II
SWITCHING STATES OF THE BRIDGE-CELL SWITCHES

State	S_1	S_2	S_3	S_4	V_{cell}
1	1	0	0	1	$+V_c$
2	0	1	0	1	0
3	1	0	1	0	0
4	0	1	1	0	$-V_c$

A. DSCC - States of Switches

As observed in Fig. 1(b), it can be verified that the switches of the chopper-cell have two states, as is verified in Tab. I. These states allow the voltage synthesized by each cell (V_{cell}) to be $+V_c$ or 0.

Therefore, it is possible to compare the normalized voltage reference signals of the upper and lower arms with the carrier signals using PS-PWM. The comparison between normalized signals can be seen in Fig. 3. Fig. 4 exemplifies for N = 4 the reference signals of the upper and lower arms with the $\beta = \frac{\pi}{2}$ displacement carriers.

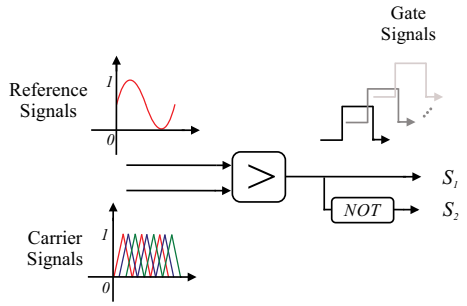

Fig. 3. PS-PWM modulation of the DSCC.

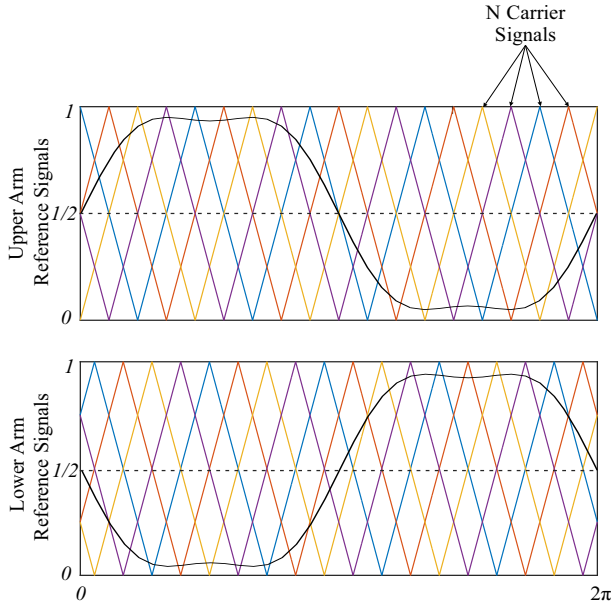

Fig. 4. Operation of PS-PWM for DSCC and DSBC-2L.

B. DSBC - States of Switches

As observed in Fig. 1(c), it can be verified that the switches of the bridge-cell have four states, as is verified in Tab. II. These states allow the voltage synthesized by each cell (V_{cell}) to be $+V_c$, 0 or $-V_c$.

In the literature, some works present the DSBC-2L topology in which the switches work only in the first two states. For this case, the amplitude of the carriers and the references of the upper and lower arms are the same as in the DSCC, as in Fig. 4. The comparison between normalized signals is performed as proposed in [18], using the unipolar modulation strategy, as illustrated in Fig. 5(a).

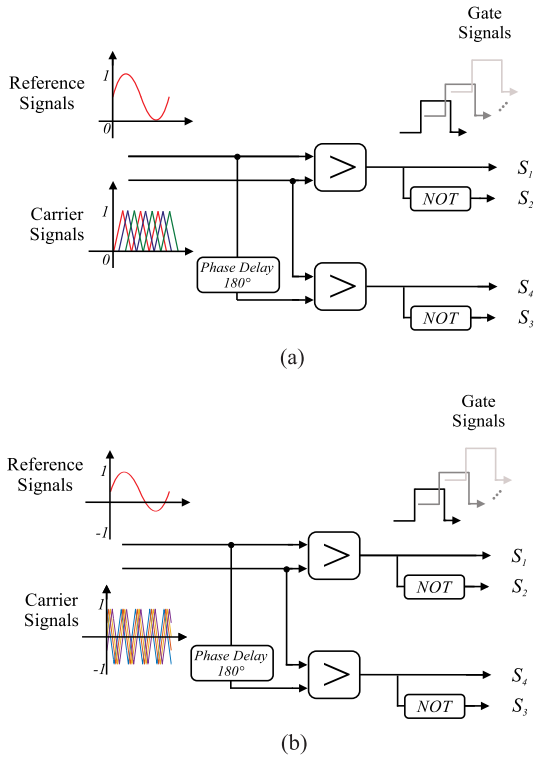

Fig. 5. PS-PWM modulation: (a) DSBC-2L; (b) DSBC-3L.

On the other hand, the DSBC-3L topology employs the four switching states, and can also synthesize the voltage $-V_c$. The comparison between normalized signals can be seen in Fig. 5(b). The unipolar modulation strategy is also used. For such comparison the arm voltage references and the carriers have amplitudes between -1 and 1, as shown in Fig. 6, for N = 4 cells per arm.

V. CASE STUDY

The case study presented in this work is based on a 15 MVA STATCOM connected to a 13.8 kV grid. The design of DSCC and DSBC-2L topologies employs the methodology proposed in [15]. In such conditions, the necessary effective dc-link voltage is 25 kV. In order to use 3.3 kV semiconductor devices, 16 cells are necessary. Therefore, the voltage per cell is 1.56 kV. For the capacitor design, the energy storage is

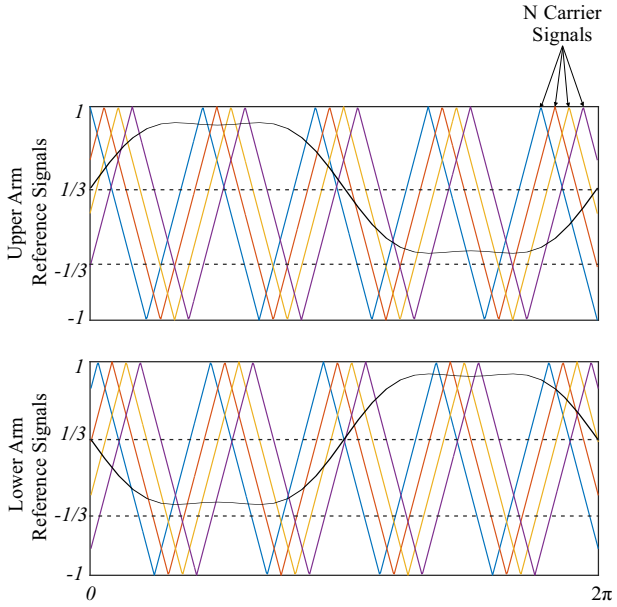

Fig. 6. Operation of PS-PWM for the DSBC-3L.

considered 40 kJ/MVA in order to guarantee 10 % of ripple at rated conditions, as suggested by [15].

For DSBC-3L topology, the dc-link voltage can be divided by two, which is an advantage in terms of insulation. The capacitor voltages is given by (3). Accordingly,

$$V'_{dc} = \frac{V_{dc}}{2}. \tag{15}$$

Therefore, in order to use the same semiconductor devices and the same cell voltage, the number of cells of DSBC-3L topology is given by:

$$v'^{*}_{cell} = v^{*}_{cell}, \tag{16}$$

$$\frac{1.5V'_{dc}}{N'} = \frac{V_{dc}}{N} \Leftrightarrow 1.5\frac{0.5V_{dc}}{N'} = \frac{V_{dc}}{N} \rightarrow N' = \frac{3}{4}N. \tag{17}$$

Therefore, the DSBC-3L presents 25 % less cells than DSCC and DSBC-2L topologies. Regarding the capacitor design, the energy storage is considered 24 kJ/MVA in order to guarantee 10 % of ripple at rated conditions.

The parameters of the designed DSCC, DSBC-2L and DSBC-3L MMC STATCOM are presented in Tab. III. The controller parameters are shown in Tab. IV. The proportional integral controllers are discretized by Tustin method, while the proportional resonant controllers are discretized by Tustin with prewarping method. These parameters were based in [15].

The case study considers three operational conditions, as illustrated in Fig. 7 and described bellow:

- $0 \leq t \leq$ 1s: -1 pu of reactive power is injected into the power grid (Capacitive Operation) and active power is zero;
- $1 < t \leq$ 1.5s: reactive power increases at a rate of 4pu/s until reaching 1pu and active power is zero;
- $1.5 < t \leq$ 2.5s: 1 pu of reactive power is injected into the power grid (Inductive Operation) and active power is zero.

TABLE III
PARAMETERS OF THE MODULAR MULTILEVEL CONVERTER

Parameters	Topologies	
	DSCC and DSBC-2L	***DSBC-3L***
Grid voltage (v_g)	$13.8kV$	$13.8kV$
Grid frequency (f_g)	$60Hz$	$60Hz$
Pole to pole dc voltage (V_{dc})	$25kV$	$12.5kV$
Rated power (S_n)	$15MVA$	$15MVA$
Arm inductance (L_{arm})	$5.1mH$	$5.1mH$
Arm resistance (R_{arm})	0.065Ω	0.065Ω
Cell capacitance (C)	$5.12mF$	$4.1mF$
Nominal cell voltage (v^{*}_{cell})	$1.56kV$	$1.56kV$
Switching frequency (f_{sw})	$270Hz$	$270Hz$
Number of cells (N)	16	12

TABLE IV
PARAMETERS OF THE CONTROLLERS

Parameters	DSCC and DSBC
Sampling frequency	$9720Hz$
Prop. gain of circulating current control	3.25
Resonant gain of circulating current control	1000
Circulating current LPF cut-off frequency	$8Hz$
Prop. gain of individual balancing control	0.0004
Prop. gain of average control	9.7
Integ. gain of average control	165.5
Prop. gain of grid current control	8.09
Resonant gain of grid current control	1000
Moving average filter frequency	$30Hz$

In order to compare the topologies, the dynamics presented in the capacitor voltages, the circulating current and the output power are analyzed. Another factor analyzed refers to Total Demand Distortion (TDD) of the output current, in order to verify the power quality. The TDD analysis is made following the IEEE Std 519-2014 [19]. In this recommendation, the TDD accounts the ratio of the root mean square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding inter harmonics, expressed as a percent of the maximum demand current. In addition, power losses in the semiconductors devices are also evaluated.

Furthermore, in order to evaluate the economic costs considering the cell capacitance, the total energy stored is calculated. The minimum value of the nominal energy storage per arm, is given by:

$$E_{nom} = \frac{CNv^2_{cell}}{2}. \tag{18}$$

The total energy storage in the MMC is $6E_{nom}$. The cost of the capacitors of the converters is approximated from

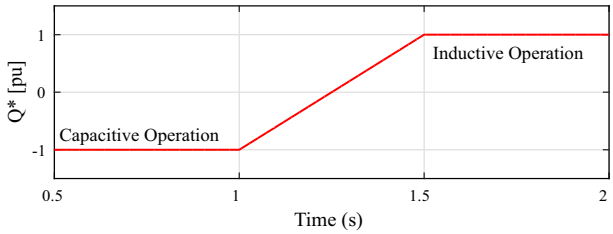

Fig. 7. Reactive power dynamic.

the current market prices and is considered as 150 €/kJ, according to [20].

The cost of the semiconductor devices, controls, cabinets, among others of the converters is approximated from the market prices and it is considered as 3.5 €/kVA, of the installed switching power P_{switch}, which is defined as [20], [21]:

$$P_{switch} = N_{semi} U_{block} I_{nom}. \tag{19}$$

The simulations were developed in the PLECS environment for validate the comparison among the topologies studied. In order to compare the thermal behavior of semiconductors in the cell, the thermal model is developed [15], considering the ambient temperature equal to $40°C$ and the maximum heat sink temperature equal to $70°C$. An ABB IGBT part number 5SND 0500N 330300 of 3.3 kV-500 A was chosen for this application.

VI. Results

Fig. 8 illustrates the capacitor voltages for the three topologies studied in this work. For both the ripple is presented in more detail for capacitive and inductive operation. In both topologies, the voltage ripple of the capacitors remained within the limit of 10 % of voltage tolerance. For the capacitive and inductive operations, the average value is represented by AVG. This value must be within the established tolerance limits of ± 10 % of v^*_{cell}.

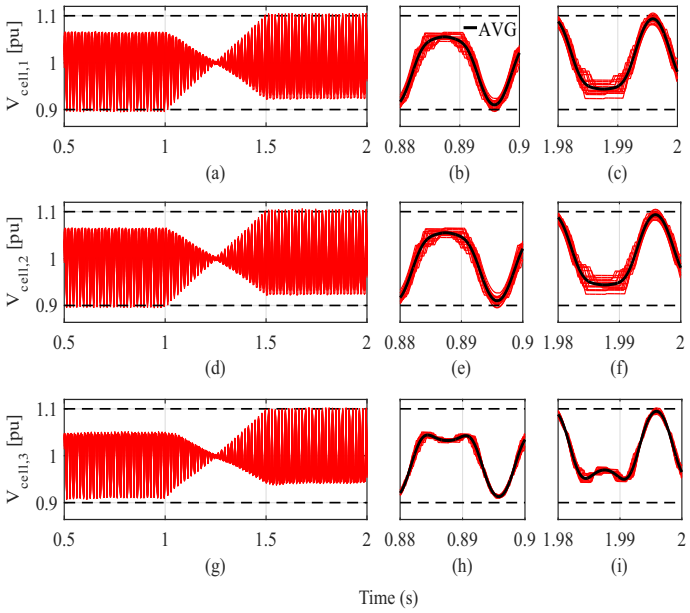

Fig. 8. Capacitors Voltage: (a) DSCC; (b) detail in capacitive operation of DSCC; (c) detail in inductive operation of DSCC; (d) DSBC-2L; (e) detail in capacitive operation of DSBC-2L; (f) detail in inductive operation of DSBC-2L; (g) DSBC-3L; (h) detail in capacitive operation of DSBC-3L; (i) detail in inductive operation of DSBC-3L.

The dynamic response and the difference among the maximum and minimum peak of the circulating current can be observed in Fig. 9. As noted, DSBC-3L presents a higher ripple in the capacitive and inductive operations, being 1.26 times larger than DSCC and 1.32 times larger than DSBC-2L. This is due to the reduction of the number of cells.

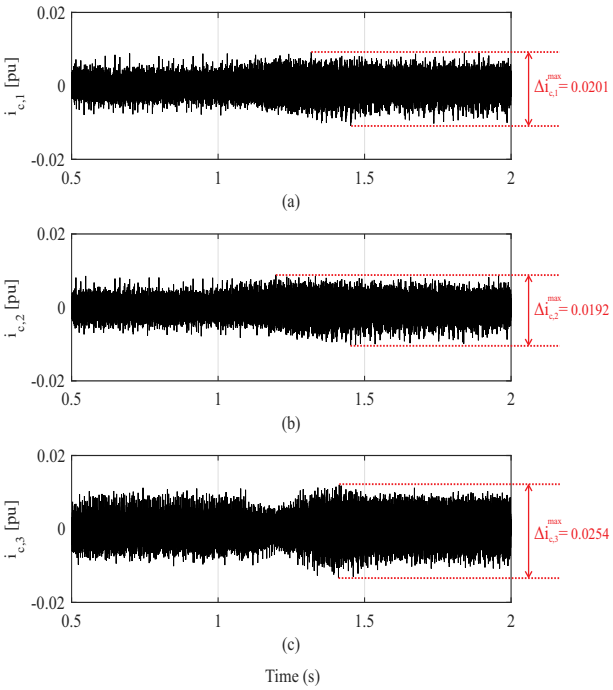

Fig. 9. Circulating current: (a) DSCC; (b) DSBC-2L; (c) DSBC-3L.

The active and reactive power of the grid is shown in Fig. 10. For the three topologies presented, the oscillation in the power response is small. However, due to the increase of the number of cells in the DSBC-3L, this topology presents higher oscillation than the other two topologies. Indeed, as shown in Fig. 11 and Fig. 12, the DCBC-3L has the highest value of reactive power absolute error in relation to the reference capacitive and inductive operations, which 0.0393pu and 0.0515pu, respectively.

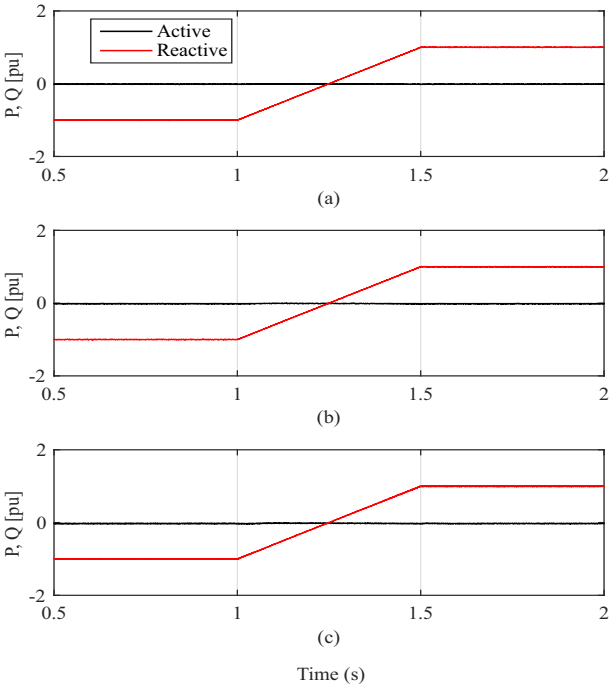

Fig. 10. Output power measured: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

Tab. V shows the TDD of the output current of the studied

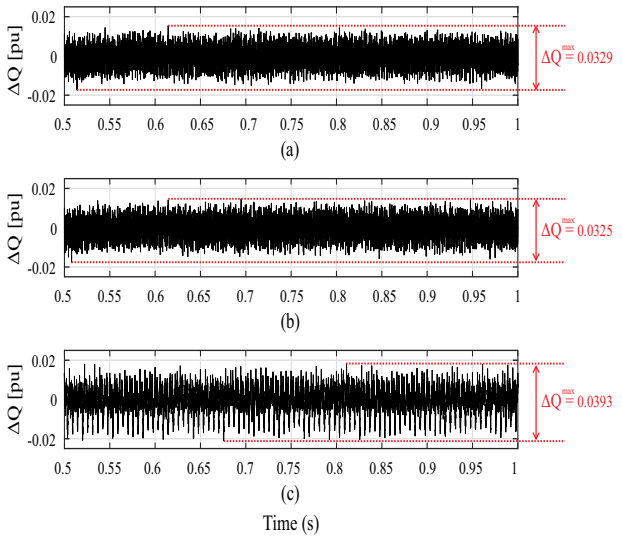

Fig. 11. Reactive power absolute error in the capacitive operation: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

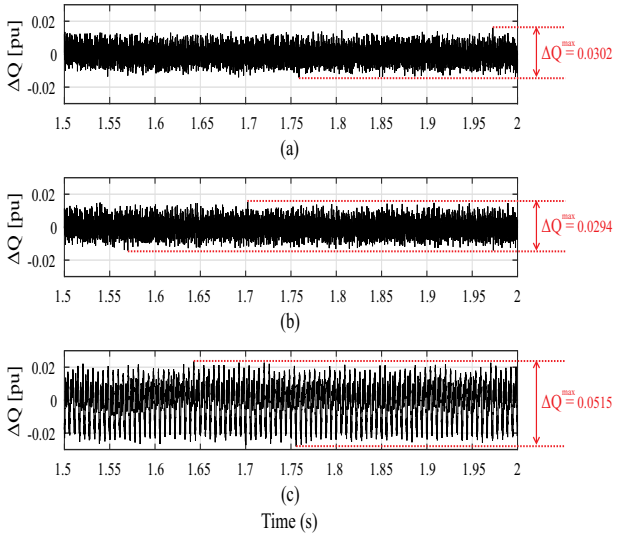

Fig. 12. Reactive power absolute error in the inductive operation: (a) DSCC; (b) DSBC-2L; (c) DCBC-3L.

topologies. For DSBC-3L the value is higher than the others, which presented similar values. The TDD value of the DSBC-3L can be explained by the increase of the circulating current while compared of the other topologies due to the decrease of the number of cells. However, both topologies fall into the recommendation proposed in [19] to a maximum of 5 %.

TABLE V
TOTAL DEMAND DISTORTION (%) OF OUTPUT CURRENT

Topologies	Capacitive	Inductive
DSCC	0.37	0.35
DSBC-2L	0.36	0.35
DSBC-3L	0.76	1.08

The power losses of the MMC are also evaluated, as shown in Fig. 13. The analyzed MMC topologies are compared in terms of conduction and switching losses in the power devices. For both capacitive and inductive operation, the power losses are similar. The topologies, the DSBC-2L presents almost two times higher power losses due to the higher number of semiconductor devices when compared to the DSCC topologies. The DSBC-3L has power losses between those presented in the other two topologies.

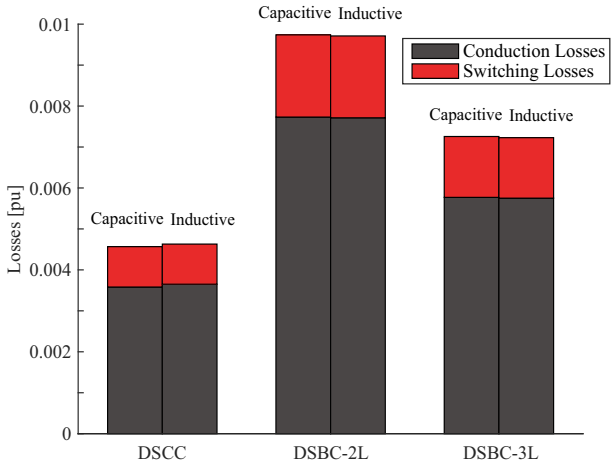

Fig. 13. Comparison of switching and conduction losses of the studied MMC topologies.

Finally, the estimated costs are shown in Tab. VI. It is possible to verify that the cost in relation to the capacitors is the same for DSCC and DSBC-2L because both topologies present the same energy storage requirement. In the DSBC-3L the total stored energy required is smaller, resulting in lower costs. Regarding the costs of power electronics, the DSBC-2L presents a higher value when compared to the other two cases due to the greater number of semiconductor devices in its design. The DSBC-3L shows costs of semiconductors between those presented in the other two topologies.

TABLE VI
ECONOMIC EVALUATION

Topologies	$6E_{nom}$	P_{switch}	Investment Costs
DSCC	600 kJ	576 MVA	1 pu
DSBC-2L	600 kJ	1152 MVA	1.96 pu
DSBC-3L	360.2 kJ	864 MVA	1.46 pu

Because the pole-to-pole voltage of the DSBC 3L is half the bus value of the DSCC and DSBC-2L, the insulation costs are lower. However, this paper does not include cost analysis in relation to this requirement.

Based on the results presented, Tab. VII summarizes the requirements considered important for comparison of the three topologies studied, where "++" denotes good characteristics, "+" denotes acceptable characteristics and "-" denotes poor characteristics.

VII. CONCLUSION

In this work, three topologies (DSCC, DSBC-2L and DSBC-3L) are compared in terms of operational characteristics for a STATCOM system, considering a 15 MVA MMC connect to a 13.8 kV grid.

Based on the operating characteristics, costs and losses, associated with the steady-state operation of the MMC was verified. In this way, the circulating current shown a small

TABLE VII
REQUIREMENTS OF THE TOPOLOGIES

Requirements	DSCC	DSBC-2L	DSBC-3L
Number of Semiconductors Devices	++	-	+
Power Losses	++	-	+
Number of Cells	+	+	++
Economic Costs of Capacitors	+	+	++
Economic Costs of Semiconductors Devices	++	-	+
Economic Costs of Insulation Bus	+	+	++
Capacity of dc Fault Blocking	-	++	++

ripple for the both topologies presenting a slightly larger ripple on the DSBC-3L. In terms of current distortion, there is more harmonic distortion in the output current for the DSBC-3L, when compared to the others, but the three topologies has TDD according to IEEE Std 519-2014. In terms of losses, the DSCC topology presented the lowest loss and the DSBC-2L presented the highest loss. The DSBC-3L has intermediate characteristics when compared to the other two topologies. Also, for the cost analysis, the same logic is observed.

Therefore, this work validated that the structure DSBC-3L presented intermediate characteristics when compared the topologies DSCC and DSBC-2L in terms of costs, dynamics and losses. When the DSBC-2L and DSBC-3L topologies were compared, the latter proved to be promising under the presented application conditions, which reveals its importance in studies and future applications in physical systems.

REFERENCES

[1] P. K. Dhal and C. C. A. Rajan, "Design and analysis of STATCOM for reactive power compensation and transient stability improvement using intelligent controller," Conf. on Electronics and Communication Systems, 2014, pp. 1-6.

[2] Y. Ma, A. Huang and X. Zhou, "A review of STATCOM on the electric power system,"Int. Conf. on Mechatronics and Automation, 2015, pp. 162-167.

[3] M. Pereira, D. Retzmann, J. Lottes, M. Wiesinger and G. Wong, "SVC PLUS: An MMC STATCOM for network and grid access applications," IEEE Trondheim PowerTech, 2011, pp. 1-5.

[4] E. Kontos, G. Tsolaridis, R. Teodorescu and P. Bauer, "High Order Voltage and Current Harmonic Mitigation Using the Modular Multilevel Converter STATCOM," in IEEE Access, vol. 5, pp. 16684-16692, 2017.

[5] R. Sartorio Camargo, W. Totola Nunes, D. Marins Dallapicula, L. Frizera Encarnacao and D. Savio Lyrio Simonetti, "Design and Analysis Methodology for Modular Multilevel Converters (MMC)," in IEEE Latin America Trans., vol. 16, no. 4, pp. 1105-1112, April 2018.

[6] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," Int. Power Elec. Conf., 2010, pp. 508-515.

[7] J. Zhang and C. Zhao, "The Research of SM Topology With DC Fault Tolerance in MMC-HVDC," in IEEE Trans. on Power De., vol. 30, no. 3, pp. 1561-1568, June 2015.

[8] A. Allu, M. Odavic and K. Atallah, "Design considerations of a full bridge modular multilevel converter under variable DC link voltage," Energy Conversion Cong. and Exp., 2017, pp. 504-510.

[9] L. He, K. Zhang, J. Xiong, S. Fan and Y. Xue, "Low-Frequency Ripple Suppression for Medium-Voltage Drives Using Modular Multilevel Converter With Full-Bridge Submodules," in IEEE Journal of Emerging and Sel. Top. in Power Elec., vol. 4, no. 2, pp. 657-667, June 2016.

[10] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," in IEEE Trans. on Power Elec., vol. 24, no. 7, pp. 1737-1746, July 2009.

[11] B. Li, R. Yang, D. Xu, G. Wang, W. Wang and D. Xu, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters," in IEEE Trans. on Power Elec., vol. 30, no. 1, pp. 297-310, Jan. 2015.

[12] K. Ilves, L. Harnefors, S. Norrga and H. P. Nee, "Analysis and Operation of Modular Multilevel Converters With Phase-Shifted Carrier PWM," in IEEE Trans. on Power Elec., vol. 30, no. 1, pp. 268-283, Jan. 2015.

[13] K. Fujii, U. Schwarzer and R. W. De Doncker, "Comparison of Hard-Switched Multi-Level Inverter Topologies for STATCOM by Loss-Implemented Simulation and Cost Estimation," Power Elec. Specialists Conf., 2005, pp. 340-346.

[14] Akagi, H., Watanabe, E. H. and Aredes, M. The instantaneous power theory. Hoboken: Wiley-IEEE Press, 2007.

[15] A. F. Cupertino, J. V. M. Farias, H. A. Pereira, S. I. S. Junior and R. Teodorescu, "DSCC-MMC STATCOM Main Circuit Parameters Design Considering Positive and Negative Sequence Compensation," 2018 Journal of Control, Automation and Elec. Sys., pp. 62-74.

[16] J. Lamb, B. Mirafzal and F. Blaabjerg, "PWM Common Mode Reference Generation for Maximizing the Linear Modulation Region of CHB Converters in Islanded Microgrids," in IEEE Trans. on Ind. Elec., vol. 65, no. 7, pp. 5250-5259, July 2018.

[17] A. Mora, J. Juliet, A. Santander and P. Lezana, "Dead-Time and Semiconductor Voltage Drop Compensation for Cascaded H-Bridge Converters," in IEEE Trans. on Ind. Elec., vol. 63, no. 12, pp. 7833-7842, Dec. 2016.

[18] Y. Xia and R. Ayyanar, "Comprehensive comparison of THD and common mode leakage current of bipolar, unipolar and hybrid modulation schemes for single phase grid connected full bridge inverters," Applied Power Elec. Conf. and Exp., 2017, pp. 743-750.

[19] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," in IEEE Std 519-2014 (Revision of IEEE Std 519-1992), pp.1-29, June 11 2014.

[20] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge and R. W. De Doncker, "Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids," in IEEE Trans. on Power Elec., vol. 30, no. 1, pp. 124-137, Jan. 2015.

[21] H. A. B. Siddique, A. R. Lakshminarasimhan, C. I. Odeh and R. W. De Doncker, "Comparison of modular multilevel and neutral-point-clamped converters for medium-voltage grid-connected applications," Int. Conf. on Renewable Energy Research and Applications, 2016, pp. 297-304.