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PERFORMANCE COMPARISON OF DIFFERENT POWER MODULES APPLIED IN PHOTOVOLTAIC INVERTERS DURING HARMONIC CURRENT COMPENSATION

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***Abstract* – The increasing of PV systems connected to distribution system affect significantly the grid power stability. Some works propose to use the PV inverter excess capacity to support harmonic compensation. The main drawback of this solution is the increase of losses in the converter during the execution of this task. Therefore, this paper analyzes the power losses in the PV inverter components (semiconductor switches and diodes) during the harmonic compensation process. Simulations considering a 5kW three-phase PV inverter are performed with focus on conduction and switching losses.**

***Keywords* – Multifunctional Operation, Harmonic Current Compensation, Power Losses, Semiconductors Devices.**

I. INTRODUCTION

In the last decade, photovoltaic (PV) power systems have experienced fast growth around the world. Predictions show that solar energy will grow by 20% per year until 2020 and solar power prices are rapidly falling to the point where solar became cheaper than on-shore wind power. Moreover, PV power systems already contribute to a good share of electrical power in many countries, such as Italy, Germany and Greece [1].

Although the benefits of PV systems are many, they are seen as not entirely exploited, since the system does not work at all during nighttime and does not work on full capacity during low profile irradiance. Due to this fact, multifunctional inverters are being studied to work on ancillary services, therefore making better usage of the installed solar power system and improving the quality of the power connected into the grid [2]. Among these ancillary tasks are reactive power injection, harmonic current compensation and frequency regulation.

Studies on techniques to execute harmonic current compensation using multifunctional inverters progressed and different methods have been tested [3]. Furthermore, inverters are a critical point of PV systems and are often the cause of failures. The failure of an inverter might happen in any component. However, the switches have showed a great level of vulnerability [4]. The switch of an inverter (usually an IGBT – Insulated Gate Bipolar Transistor or a MOSFET – Metal-Oxide Semiconductor Field-Effect Transistor) is affected by thermal stress, electrical stress, mechanical stress and other factors. The switches of ancillary multifunctional inverters are specially affected by the extra work, being the thermal stress the main source of the wear of the devices, leading researchers to worry about the reliability of the system over its lifetime [5], [6]. Therefore, studies on how the extra task of harmonic current compensation affects the inverter's switches are needed.

As mentioned, Si IGBTs are widely used as semiconductor devices in inverters. Recently, Silicon Carbide (SiC) MOSFETs emerged as an alternative to IGBTs, especially for high power applications [7]. SiC based devices present low conduction loss, higher switching frequencies and higher voltage capability than traditional Si Devices. SiC MOSFETs have been compared to IGBTs on inverter applications, showing that they can perform better than the traditionally used device [8]. However, these tests have not been performed when inverters are doing harmonic current compensation. In order to study the impact of ancillary work on inverters, this paper investigates the power losses in the PV inverter switches, performing harmonic current compensation. The harmonic detection method used in the tests is the SOGI PLL method, due to its improvement in the harmonic detection over other methods [12]. A Cree SiC MOSFET and two Infineon Si Trench IGBT, of third and fourth generation, are compared. The thermal model of the devices is simulated on PLECs to check how they work under different switching frequencies and power conditions. The switching frequencies are 12 kHz, 36 kHz and 48 kHz while a 5^{th} harmonic of 5A of magnitude is compensated. The results compare the efficiency and the thermal stress for each solution.

By comparing the devices, this paper contributes to the development of multifunctional inverters and to further studies, in order to allow PV inverter perform ancillary tasks, improving the power system stability.

II. METHODOLOGY

In order to compare the semiconductors switching devices during harmonic compensation, this paper uses a single-phase PV multifunctional inverter. The main function of the inverter is to convert the dc power generated by the solar panels in ac and inject it into the grid. In addition, it compensates harmonic current components from loads connected in the power system. This topology is shown in Fig. 1.

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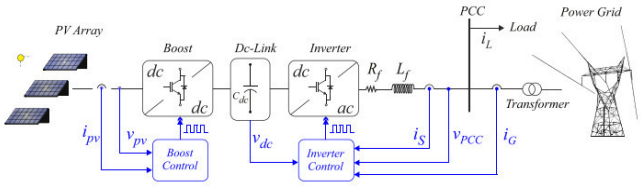

Fig. 1. Single-phase grid-connected photovoltaic system.

A. Control Strategy

The control strategy implemented is based in two cascaded loops: inner control loops; controlling the injected direct and quadrature currents, and the outer control loops; controlling the dc bus voltage and the reactive power injected into the grid [13]. To ensure system synchronization, a Phase- Locked Loop (PLL) structure is used in order to synchronize the system. The detailed control schematic is shown in Fig. 2.

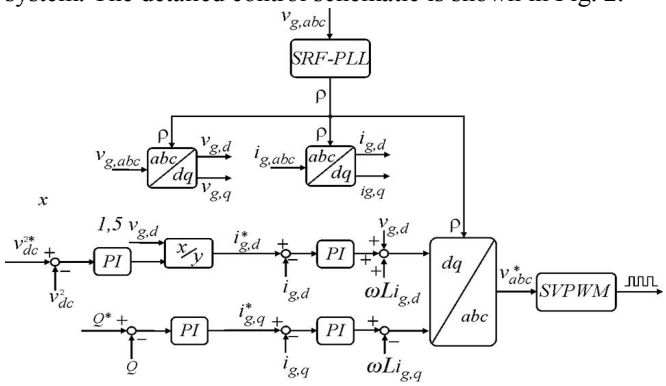

Fig. 2. Detailed control schematic.

In the inner control strategy, the direct and quadrature axis current, and the closed-loop transfer function is given by:

$$\frac{I_{d,q}(s)}{I^*_{d,q}(s)} = \frac{1/R}{L/R\,s\,+1}\,k_{i1}\frac{(\frac{k_{p1}}{k_i}s+1)}{s} \qquad (1)$$

where $R = R_f + R_g$ and $R = L_f + L_g$, from the equivalent simplified circuit of the ac side inverter. The inner loop parameters are presented in Table I.

TABLE I
Control parameters

Variable	Description	Value
V_g	Grid voltage	220 V
L_f	LCL filter inductor	1.5 *mH*
C_f	LCL filter capacitor	8.71 µF
C_{bus}	Dc-link capacitance	1 mF
R_d	Damping resistance	0.4 Ω
L_g	Grid-side inductor	1.5 mH
$k_{p,bus}$	Dc-link controller proportional gain	0.1131
$k_{i,bus}$	Dc-link controller integral gain	3.5530
$k_{p,pll}$	PLL proportional gain	0.5728
$k_{i,pll}$	PLL integral gain	50.8958

The outer control loop is divided into reactive power control and dc-link voltage control. In equation (2) it is shown the transfer function of the reactive power loop PI control.

$$\frac{Q(s)}{Q^*(s)} = \frac{1+T_1\,s}{1+T_2\,s}\,k_{i1}\frac{(\frac{k_{p1}}{k_i}s+1)}{s} \qquad (2)$$

where $T_2 = \frac{1+Hk_{p2}}{Hk_{i2}}$, $T_1 = \frac{k_{p2}}{k_{i2}}$ and $H = -\frac{3}{2}\,v_g$.

For the dc-link voltage control, the dynamic equation of the square of dc-bus voltage is given by:

$$\frac{dv^2{}_{dc}}{dt} = \frac{2(P_{PV}-P_C)}{C_{dc}} \qquad (3)$$

where P_{PV} is the active power generated by solar panels and P_C is the active power drawn by the converter.

Applying Laplace transform in (3), the close-loop considering a PI controller is given by:

$$\frac{V^2{}_{dc}}{V^{*2}{}_{dc}} = \frac{2(s\,k_{p,bus}+\,k_{i,bus})}{Cs^2+2(s\,k_{p,bus}+\,k_{i,bus})} \qquad (4)$$

In the case of the inner loop, the parameters of the outer loop are presented in Table I.

In the harmonic current detection process, the SOGI-PLL structure is used. In this detector, there is a first stage that detects the fundamental component of the load current. The remaining signal consists of the harmonics components. The next stages estimate the harmonic currents according to the largest amplitude. Each stage is composed by a Second-Order-Generalized-Integrator (SOGI-PLL) structure. The SOGI-PLL structure is illustrated in Fig. 3.

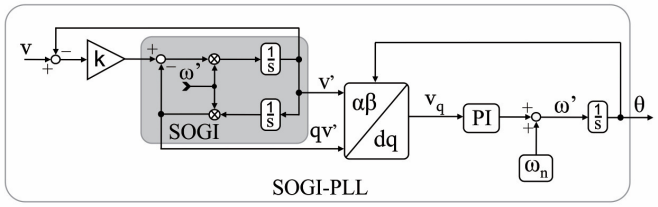

Fig. 3. SOGI-PLL Structure.

In order to improve the performance of the harmonic current detector, a negative feedback strategy control is applied [12]. The negative feedback method is the return of part of an output signal to the input, so the output is improved.

The current control is done by means of multi-resonant proportional controllers (PMR) dynamically adjusted in each harmonic frequency to be compensated. The transfer function of the PMR can be represented by:

$$G_c(s) = K_P^r + \sum_{h=1}^{n} K_{i,h}^r\,\frac{s}{s^2+\,\omega_h^2}, \qquad (5)$$

where K_P^r is the proportional gain, h is the harmonic order $(h = 1,2,3,\ldots,n)$, w_h are the resonance frequencies and $K_{i,h}^r$ are the integrated gains.

B. Switches Characteristics and Losses Calculations

One of the best advantages of SiC MOSFETs compared to Si IGBTs is its fast switching and low switching losses capability [9]. These advantages are especially considerable

for high power, high switching applications, such as in solar power inverters.

1) SiC MOSFET and IGBT Characteristics: In order to compare IGBTs and MOSFETs, similar devices were selected. The main characteristics of the chosen devices are presented on Table 2.

TABLE II
Devices specifications

	Device		
	SiC MOSFET 2^{nd} Generation	**IGBT 3^{rd} Generation**	**IGBT 4^{th} Generation**
Maker	Cree	Infineon	Infineon
Part Number	CCS020M12CM2	FS25R12KT3	FS25R12W1T4
Rated Voltage	1.2 kV	1.2 kV	1.2 kV
Rated Current	20 A	25 A	25 A
Notation in this Paper	M2	T3	T4

Also, an important characteristic in SiC MOSFET is the reducing of the temperature sensitivity by high speed switching due to the presence of parasitic inductance [15].

2) Losses: The losses in a semiconductor component can be divided in two categories: conduction and switching losses [13]. Conduction losses occur when the circuit requires the current and the voltage at its terminals is the voltage drop due to the device itself. In the other hand, switching losses occur when the device is transitioning from the blocking state to the conducting state and vice-versa.

In order to calculate the total power losses in this work, the data from datasheets of the respective semiconductor component was considered and a lookup table was created in PLECs environment. Therefore, the power losses can be obtained for any operation condition of the semiconductor switch. The conduction and switching losses data are showed in Fig.4 and Fig.5 respectively. It is important to note that for the curves of the datasheets there are some test conditions that were taken into account, such as gate resistance, inductance, collector emitter voltage, gate source voltage, drain source current, among others. These test specifications can be found on the datasheet of the components presented in Table II.

One limitation of the analysis proposed in this work is the influence of the converter layouts in switching losses, which is not approached. Nevertheless, the methodology employed here can be used for a first evaluation. The exactly estimation of the losses is beyond the scope of this work.

C. *Thermal Model*

In the literature, it is known the electrical performance of a device is directly related to its thermal behavior through the power losses [14]. The main source of temperature rise in electronic devices are the power losses composed by the conduction and switching losses.

The range of operating temperature of the device is necessary to estimate its lifetime and power losses. In order to study the losses inside the semiconductors components, a thermal model which estimates the junction temperature is used. In the heatsink model, the thermal capacitance was not considered and the initial temperature adopted was 40ºC. The thermal model and the power losses for the IGBT/MOSFET are obtained from the datasheets. The thermal data was taken from the datasheets of the IGBTs, SiC MOSFET and the diodes. Thereafter, their respective Foster thermal model was generated on PLECs simulator.

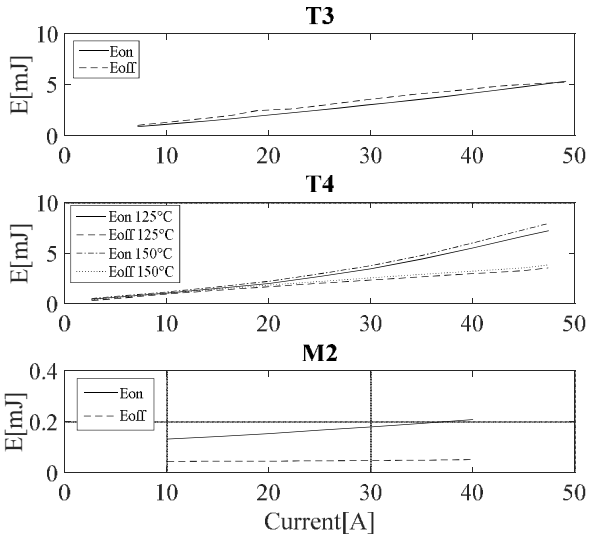

Fig. 4. Switching Losses

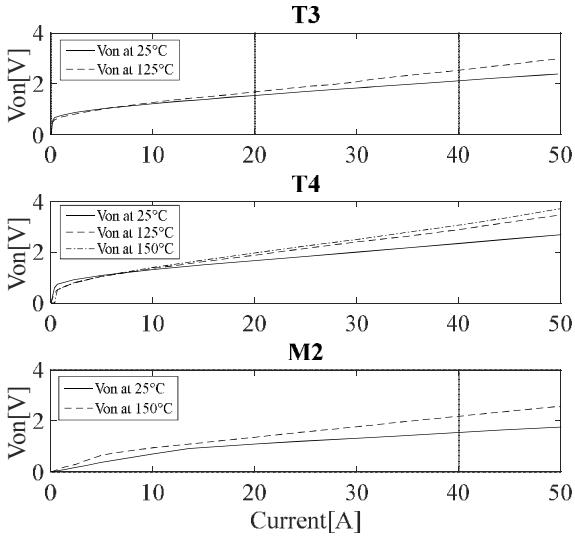

Fig. 5. Conduction Losses

III. CASE STUDY

In order to compare the efficiency of the semiconductors switches in a PV inverter applied to harmonic compensation, this paper simulates a 5 kW single-phase inverter as showed in Fig.1. The inverter used can work as multifunctional operation mode; it is able to inject active power into the grid and compensate harmonic current components as well. The model was simulated on PLECs.

A nonlinear load is used to simulate the injection of the harmonic components into the grid. In this work, a 5th harmonic component of 5 A of amplitude and phase 0 are injected. It is used a harmonic current source with phase 0º, because it is the worst case scenario. The SOGI-PLL using negative feedback is able to detect harmonic components with the highest amplitude (5th in this case study) and compensate it, improving the quality of the generated power. Also, the Tustin-Tustin discretization method was used to discretize the SOGI-PLL.

The strategy control showed in the methodology of this paper was applied. A radiation of 500 W/m$^{2.}$ was simulated. The PV panel specifications and the simulation parameters are shown in TABLE III and IV, respectively.

TABLE III
PV PANEL SPECIFICATIONS

Parameters	Values
Nominal Power	250 W
Short Circuit Nominal Current (I_{scn})	8.5 A
Open Circuit Nominal Voltage (V_{ocn})	35.5 V
Maximum Power Point Current (I_{mp})	7.99 A
Maximum Power Point Current (V_{mp})	31.29 V

TABLE IV
SIMULATIONS PARAMETERS

Parameters	Values
Switching Frequency	12 kHz
Sampling Frequency	12 kHz
PCC Voltage	220 V
DC -link Voltage	390 V
DC-link Capacitance	0.5mF

In order to study the power losses of the three semiconductor switches devices, the tests were divided in three cases. The difference in each case is the switching frequency, which is 12 kHz for Case 1, 36 kHz for Case 2 and 48 kHz for Case 3, as shown in Table V. The simulation was run for 2.0 seconds for each case and the harmonic current compensation starts at 0.8 seconds. Therefore, the losses due to harmonic current compensation are calculated after 0.8 seconds. In addition, the filter parameters depend on the switching frequency. Thus, those parameters are recalculated when the switching frequency changes.

TABLE V
Case studies implemented

Case	f_{sw}
1	12 kHz
2	36 kHz
3	48 kHz

IV. RESULTS

In the results, the conduction losses and switching losses were compared for Case 1. Then, the total losses and the losses caused by harmonic compensation will be compared in cases 1, 2 and 3.

A. *Conduction Losses*

The conduction losses in the switches for Case 1 are shown on Fig. 6. When the system stabilizes, T4 has the highest losses, followed by T3 and M2, which has the lowest losses. When the harmonic compensation starts, the power loss increases by 1.24 W in T4, by 1.16 W in T3 and by 1.66 W in M2.

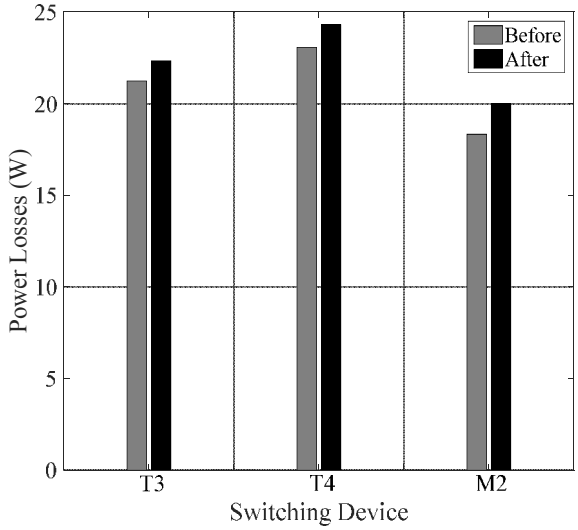

Fig. 6. Conduction Loss in the switches

B. *Switching Losses*

The Fig. 7 shows the switching losses in the switches. In this case, the losses are considerably different for the devices. T3 has the highest losses, reaching 39.34 W of losses when the device is compensating harmonics. It is followed by T4, which reaches 23.41 W in the same conditions. As it is characteristic to SiC devices, M2 has very low switching losses, losing only 1.92 W of power during harmonic current compensation.

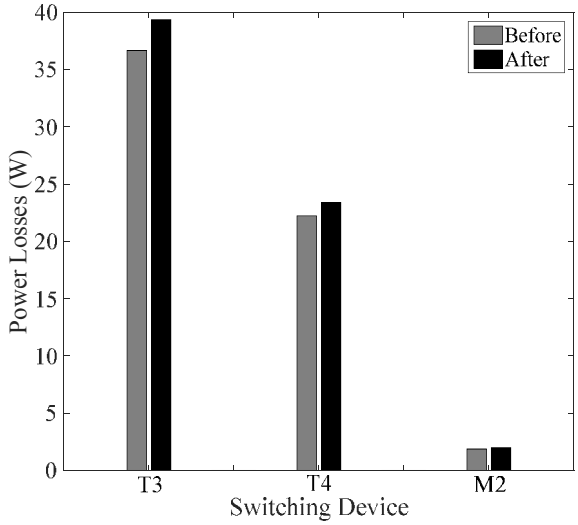

Fig. 7. Switching Loss in the switches

C. *Evaluation of cases 1, 2 and 3*

The Fig. 8 and Fig. 9 shows the overall losses in the switches for cases 1, 2 and 3. The overall losses include the switching losses and the conduction losses. In Fig. 8 the comparison makes it clear that the SiC MOSFET has the lowest losses and T3 has the highest losses for all the cases.

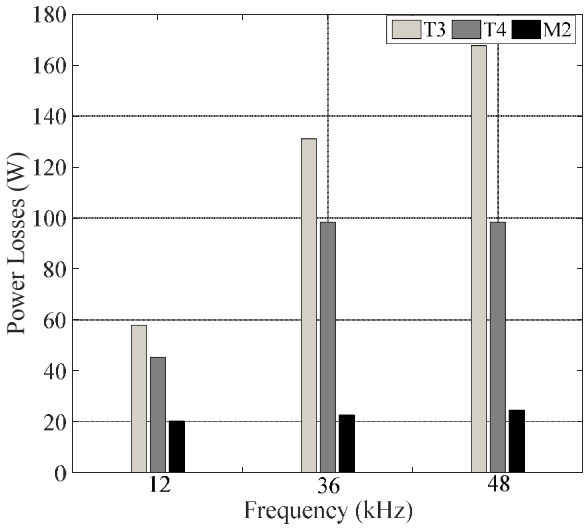

Fig. 8 - Overall losses before harmonic compensation for cases 1,2 and 3.

In Fig. 9 it is possible to infer that only a small variation in power loss occurred when the devices were not compensating harmonics. The IGBT T3 has the highest losses among the devices, following the same pattern seen in Fig. 8.

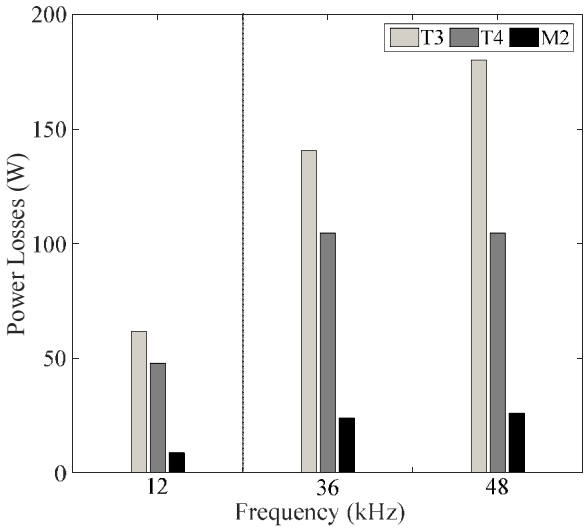

Fig. 9. Overall losses after harmonic compensation for cases 1,2 and 3.

The Fig. 10 shows the variation of power losses in the switches when they start compensating harmonics. Therefore, this figure shows the difference between the Fig. 8 and Fig. 9 and it shows the increase in power losses due to harmonic current compensation. T3 has the highest increase in losses. The increase in power losses for T3 and T4 rise with the high switching frequencies. However, for M2 this increse does not have the same behavior. It is because the temperature sensitivity is reduced by high speed switching due to the presence of parasitic inductance.

Fig. 11 shows the percentage increase in power loss for T3, T4 and M2 for cases 1, 2 and 3. It is possible to infer that although the amplitude of power loss due to harmonic compensation is different for each switch, the percentage of increase is very similar, remaining between 5% and 9% for all cases and all three devices. Again, T3, T4 and M2 follow the same behavior with high speed frequency. The reason for this is the same as discussed before.

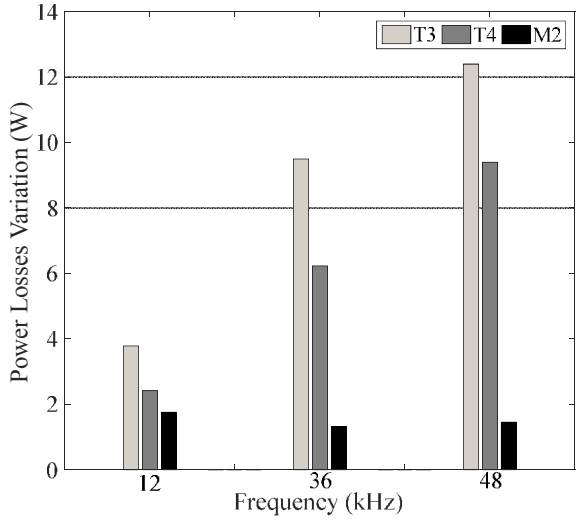

Fig. 10. Increase in power loss due to harmonic compensation

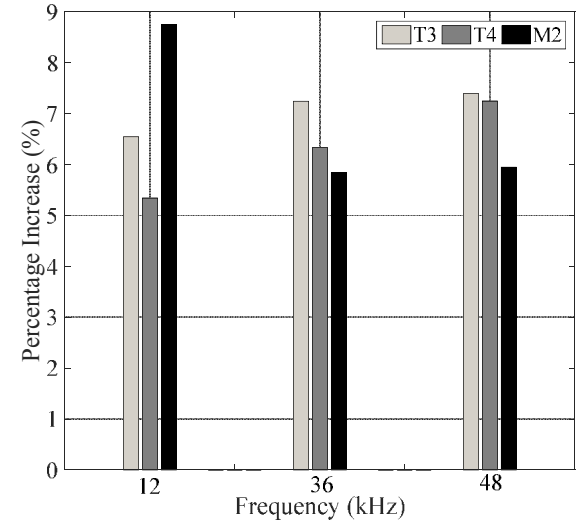

Fig. 11. Percentage increase in power loss due to harmonic compensation.

V. CONCLUSION

The obtained results show that harmonic current compensation causes an increase of power losses in the switches. M2 shows the lowest losses in all tests while T3 has the highest. The difference between M2 and the other two devices is significant and this device shows the best potential to be used on hamornic current compensation.

Although the overall losses and the losses during harmonic current compensation are the lowest in the SiC MOSFET, it is possible to infer that the percentagem increase of power losses when the system starts to performe the ancillary service is very similar to T4, T3 and M2. It means in the conditions presented in the tests the losses in the harmonic compensation are proportional to the losses without the ancillary task.

For future work, it is necessary to study the power modules losses when the inverter is compensating hamornics of phases different than zero. It will answer if the results obtained in this work are valid for different phase angles. Furthemore, it is necessary to investigate how harmonic current compensation influences the lifetime of the inverter and how it will affect the reliability of the system.

VI. ACKNOLEDGEMENTS

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