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Design and Lifetime Analysis of a DSCC-MMC STATCOM

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Abstract - **The modular multilevel converters (MMCs) has been employed in several applications as HVDC systems, energy storage, renewable energy, electrical drives and STATCOMs. In STATCOM application, the converter needs to compensate negative sequence components and unbalanced currents. Nevertheless, the design proposed in the literature considers only positive sequence compensation. Since the STATCOM is submitted to a variety of current stresses, the reliability analysis is strongly recommended. Therefore, this work presents a lifetime analysis and a design methodology considering both positive and negative sequence reactive power compensation. A case study considering a 7 MVA MMC STATCOM is analyzed in order to validate the proposed design. The lifetime consumption of the power modules employed is evaluated considering a mission profile acquired from a factory in southeastern of Brazil. Two IGBT solutions (with different current rating) are compared. The results indicate that if the power modules rated current is doubled, implying in an increase of initial cost smaller than 60 %, the lifetime of the converter can be increase until 3.6 times while the total losses are reduced in 4.4 %.**

Keywords – **MMC STATCOM, Negative and Positive Sequence Compensation, Lifetime, Reliability.**

I. INTRODUCTION

The family of modular multilevel converters (MMC) is often used in high-voltage transmission or medium-voltage distribution in several applications such as high voltage direct current (HVDC), energy storage, renewable energy, electrical drives and static synchronous compensator (STATCOM).

Regarding the STATCOM application, the converter must be able to compensate positive sequence reactive power, negative sequence reactive power and low frequency active power at the same time. Due to the capability to control the reactive power of negative sequence by having circulating current that flow inside, the double-star chopper cell (DSCC) based STATCOM [1] is used for this application.

In high power applications of DSCC-MMC STATCOM, a high number of submodules is employed, for example, a system in China operates with 1620 chopper cells, totaling 3240 semiconductors (IGBT with antiparallel diode) in the converter [2]. In the event of failure of one of the cells, generally

a redundancy technique is applied to the converter in order to avoid non-interruption of energy transfer. Nevertheless, reliability is an actual concern of power electronics in recent years.

The incompatibility of the coefficient of thermal expansion between adjacent layers in the semiconductor power modules is directly related to the operation temperature, which is one of the main reasons for the module failures [3]. Therefore, highly reliable components are required in order to minimize the downtime during the lifetime of the converter and implicitly the maintenance costs.

In view of the points aforementioned, this work provides the following contributions:

- Design of MMC based STATCOM, considering both positive and negative sequence injection;
- Semiconductor lifetime analysis of a MMC STATCOM considering a mission profile of a factory located in the southeastern region of Brazil;
- Cost, losses and lifetime comparison between two solutions of power modules with different current ratings.

II. Modular Multilevel Converter

A. Topology and Control Design

The DSCC-MMC STATCOM topology studied in this work is illustrated in Figure 1. Each SM contains a capacitance C and four semiconductor switches (S_1, S_2, D_1 and D_2). The converter is connected to the main grid through a three-phase transformer with inductance L_g. Generally, there is a switch S_T in parallel with the SM bypassing it in case of failures. The converter presents N SM per arm, i_u and i_l are the upper and lower arm currents, respectively.
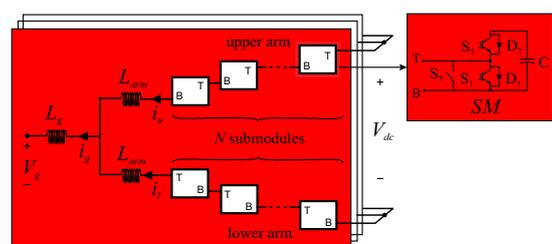
Fig. 1. : Schematic of the DSCC-MMC STATCOM.

The control strategy is presented in Figure 2. The proposed grid current control is responsible for injecting positive and negative sequence reactive power into the grid, being implemented in stationary ($\alpha\beta$) reference frame. Basically, the ex-

ternal loop controls the square of the average voltage v_{avg} of all converter SMs. This average voltage is computed by:

$$v_{avg} = \frac{1}{6N} \sum_{i=1}^{6N} v_{sm,i}, \qquad (1)$$

where $v_{sm,i}$ is the ith SM voltage.

The average voltage reference v_{avg}^* is given by:

$$v_{avg}^* = \frac{V_{dc}}{N}, \qquad (2)$$

where V_{dc} is the nominal MMC effective dc-link voltage. Although, there is no physical dc-link, this value is an important parameter to avoid overmodulation [4].
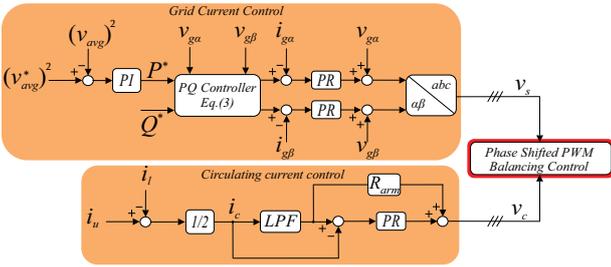
Fig. 2. : Proposed control strategy for STATCOM.

The average voltage loop calculates the necessary active power P^* that flows to the converter. Using the instantaneous power theory [5], it is possible to obtain expressions for the grid current reference by:

$$\begin{bmatrix} i_{g\alpha}^* \\ i_{g\beta}^* \end{bmatrix} = \frac{1}{v_{g\alpha}^2 + v_{g\alpha}^2} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}, \qquad (3)$$

where $v_{g\alpha}$ and $v_{g\beta}$ are the stationary components of the grid voltage.

Proportional resonant (PR) controllers are employed in order to track the reference current. The dynamics of the grid current in the stationary reference frame is given by [6]:

$$v_{s,\alpha\beta} = v_{g,\alpha\beta} + L_{eq}\frac{di_{g,\alpha\beta}}{dt} + R_{eq}i_{g,\alpha\beta}, \qquad (4)$$

where $L_{eq} = L_g + 0.5L_{arm}$, $R_{eq} = R_g + 0.5R_{arm}$ and $v_{s,\alpha\beta}$ is the equivalent output voltage of the MMC. L_{arm} and R_{arm} are the inductance and the resistance of the arm inductors, respectively.

The circulating current control is responsible for reducing the harmonics and inserting damping in the converter dynamic response. The current per leg is given by [7]:

$$i_c = \frac{i_u + i_l}{2}. \qquad (5)$$

The acting per leg of the circulating current is given by [8]:

$$v_c = L_{arm}\frac{di_c}{dt} + R_{arm}i_c, \qquad (6)$$

where v_c is the STATCOM internal voltage.

Figure 2 presents the circulating current control loop. The circulating current reference i_c^* is obtained through low-pass

filtering of i_c [8], a butterworth second order filter is employed. Whereas negative sequence injection, a considerable 2nd harmonic component appears in the circulating current, it is necessary to implement a resonant controller.

The reference voltages v_s and v_c are inputs of the modulation strategy. This paper uses the phase-shift pulse width modulation (PS-PWM) method with injection of $1/6$ of third harmonic in the phase voltages [9]. The angular displacement of the carriers is calculated by the following equation:

$$\theta_{u,n} = \pi\left(\frac{n-1}{N}\right) \quad and \quad \theta_{l,n} = \theta_{u,n} + \beta,$$

where $n = 1, 2, ..., N$. The angle β indicates the angular displacement between the carrier waveforms in the upper and lower arms.

Since in STATCOM applications the ac side power quality is preferred, the $(2N+1)-level$ modulation is employed [10]. The angular displacement in this strategy is given by:

$$\beta = 0 \quad \text{, N is odd} \qquad \beta = \frac{\pi}{N} \quad \text{, N is even}$$

In the PS-PWM method, an extra individual balancing control loop is necessary. As suggested in [7], a proportional controller k_b is employed. In this case, the individual balancing control law is given by:

$$v_b = k_b(v_{sm}^* - v_{smf,i})sign(i_{sm,i}), \qquad (7)$$

where $i_{sm,i}$ is the arm current of the ith SM. $v_{smf,i}$ is obtained from the individual capacitor voltages through a moving average filter [10]. In such conditions, the normalized reference signals per phase are given by:

$$v_{u,n} = v_b + \frac{v_c}{v_{sm}^*} - \frac{v_s}{Nv_{sm}^*} + \frac{1}{2},$$

$$v_{l,n} = v_b + \frac{v_c}{v_{sm}^*} + \frac{v_s}{Nv_{sm}^*} + \frac{1}{2}. \qquad (8)$$

B. Switching frequency

A high switching frequency increases the losses and reduces the converter efficiency. However, a larger switching frequency results in a better capacitor voltage balancing. In [10] is shown that 7/2 of the line frequency is a good choice among several values to be used for the switching frequency of the converter. Therefore, $f_c = 210\,Hz$ is employed in this work.

Since the ac component included in v_{sm} works as a disturbance in the current control system, it should be eliminated by a moving-average filter [10], the window time must be:

$$1/f_{ma} = f_n'/f_n, \qquad (9)$$

where f_n' is obtained from the irreducible fraction of the carrier frequency f_c with respect to the supply frequency f_n, denoted by f_c'/f_n'.

C. Number of SMs and semiconductor devices

In the case study proposed, a 7 MVA STATCOM with line voltage of 13.8 kV at the point of common coupling (PCC) is considered. The following considerations are assumed:

- The variations in the grid voltage are assumed 5 %;
- The STATCOM output impedance in pu is considered 14 % with a variation of 5 % around this value;
- The effective dc-link voltage presents in the worst case 10 % of ripple and a constant error of 3 % in steady-state.
- Maximum modulation index is nearly $\lambda m_{max} = 1.15$.
- Converter design considering both positive and negative sequence current compensation.

Under these conditions, the approximate value of the effective dc-link voltage is $V_{dc} = 28kV$ as suggested by [4].

The number of SMs is determined by:

$$N = \frac{1}{f_{us}} \frac{V_{dc}}{V_{svc}}, \tag{10}$$

where f_{us} is defined by the ratio between the reference voltage of SMs v_{sm}^* and the semiconductor device voltage class V_{svc}. Assuming a voltage ripple of up to 10%, $f_{us} = 0.5$ is employed. Thereby, considering semiconductors with voltage class of 3.3 kV, $N = 17$ is obtained.

Due to symmetry, only the upper arm current is verified. The maximum value for the current is given by:

$$\max(i_u) = \max(i_c) + \frac{1}{2} \max(i_g). \tag{11}$$

According [11], $\max(i_c) \leq \frac{1}{4}\lambda m_{max}\widehat{I}_n$ and $\max(i_g) \leq \widehat{I}_n$, where $\widehat{I}_n$ it is given by:

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}} \frac{S_n}{V_g}. \tag{12}$$

Thus, the maximum and rms upper arm current is:

$$max(i_u) = \left(\frac{1}{2} + \frac{\lambda m_{max}}{4}\right) \widehat{I}_n, \tag{13}$$

$$i_{u,rms} = \frac{\widehat{I}_n}{2}\sqrt{\frac{(\lambda m_{max})^2}{4} + \frac{1}{2}}. \tag{14}$$

Thus, $max(i_u) = 326A$ and $i_{u,rms} = 189A$.

D. SM capacitance and arm inductance

The SM capacitance can be designed based on the energy storage requirements of the converter. According to [9], the minimum SM capacitance is given by:

$$C = \frac{2NE_{nom}}{V_{dc}^2}, \tag{15}$$

where E_{nom} is the minimum value of the nominal energy storage per arm. Considering only the upper arm due to symmetry:

$$E_{nom} = \frac{\Delta E_{max}}{k_{max}^2 - \max(\frac{n_u^2 - e_{v,u}k_{max}^2}{1 - e_{v,u}})}, \tag{16}$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. Finally:

$$n_u = \frac{v_u}{V_{dc}}, \tag{17}$$

$$e_{v,u} = \frac{e_u}{\Delta E_{max}}. \tag{18}$$

where ΔE_{max} and e_u are the storage and variation energy.

For simplification, the grid voltage is assumed balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. Assuming the injection of $1/6$ of third harmonic component, the inserted voltages v_u can be expressed as:

$$v_u = \frac{V_{dc}}{2} - \frac{V_{dc}}{2}m \cos(\omega_n t + \theta_v) + \frac{V_{dc}}{12}m \cos(3\omega_n t). \tag{19}$$

Furthermore, the upper arm current is given by:

$$i_u = \frac{m\widehat{I}^+}{4} \cos(\varphi^+) + \frac{\widehat{I}^+}{2} \cos(\omega_n t + \varphi^+ + \theta_v)$$
$$+ \frac{m\widehat{I}^-}{4} \cos(\varphi^- + \theta_v) + \frac{\widehat{I}^-}{2} \cos(\omega_n t + \varphi^- - \theta_v). \tag{20}$$

The energy variation in the upper arm can be expressed by:

$$e_u = \int v_u i_u dt. \tag{21}$$

Thus, energy variation in the upper arm can be obtained by performing the integration:

$$e_u = \frac{S_n}{12\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2u}\right]$$
$$+ \frac{S_n}{12m\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{3u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{4u}\right] \tag{22}$$

Additionally,

$$\begin{aligned} f_{1u} &= \frac{m}{9} \cos(\varphi^+) \sin(3\omega_n t) + \frac{1}{6} \sin(2\omega_n t - \varphi^+ - \theta_v) \\ &\quad + \frac{1}{12} \sin(4\omega_n t + \varphi^+ + \theta_v), \\ f_{2u} &= \frac{m}{9} \cos(\varphi^- + \theta_v) \sin(3\omega_n t) + \frac{1}{6} \sin(2\omega_n t - \varphi^- + \theta_v) \\ &\quad + \frac{1}{12} \sin(4\omega_n t + \varphi^- - \theta_v), \\ f_{3u} &= -2m^2 \cos(\varphi^+) \sin(\omega_n t + \theta_v) \\ &\quad - m \sin(2\omega_n t + \varphi^+ + 2\theta_v) + 4 \sin(\omega_n t + \varphi^+ + \theta_v), \\ f_{4u} &= -2m^2 \cos(\varphi^- + \theta_v) \sin(\omega_n t + \theta_v) \\ &\quad - m \sin(2\omega_n t + \varphi^-) + 4 \sin(\omega_n t + \varphi^- - \theta_v). \end{aligned} \tag{23}$$

Since $\Delta E_{max} = max(e_u)$ and E_{nom} are proportional to the converter rated power, the energy storage requirements of the converter can be expressed by:

$$W_{conv} = \frac{6}{S_n} E_{nom}, \tag{24}$$

where W_{conv} is the required energy storage per MVA.

The requirement of energy storage in Figure 3 can be obtained considering the worst case, with $m = 1.15$, $k_{max} = 1.1$ and $\varphi^+ = \varphi^- = \pi/2$. The MMC capability curve is defined by the equation:

$$\widehat{I}^+ + \widehat{I}^- = \widehat{I}_n. \tag{25}$$

Taking into account the capability curve, the maximum required value of W_{conv} is approximately 38.63 kJ/MVA, as observed in Figure 3. Using this value, the SMs capacitance found by (15) is approximately $C = 2mF$. This value guarantees that the voltage ripple in steady-state is at most 10 % for any positive and negative sequences since respect the curve.
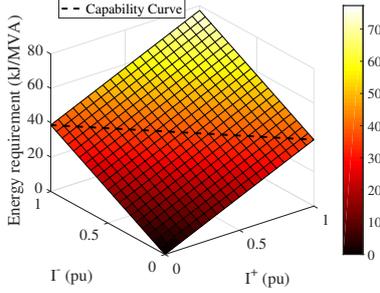
Fig. 3. : Energy storage requirements as function of positive and negative sequence current components.

Regarding the arm inductance, an important role of this component is to prevent the resonance frequency [12], once the control strategy suppresses the second harmonic component of the circulating current. In this case, the following relation must be satisfied:

$$L_{arm}C > \frac{5N}{48\omega_n^2}. \tag{26}$$

Another feature performed by the inductor is to limit the arm current during faults [13]. Whereas the worst case is a short circuit applied between the positive and negative dc-buses:

$$L_{arm} = \frac{V_{dc}}{2\alpha}, \tag{27}$$

where α (kA/s) is the maximum current rise rate.

According to (27), if $\alpha = 0.1(kA/\mu s)$ [13], the minimum value of inductance is 0.14 mH (0.004 pu). By applying (26), $L_{arm} > 6.23mH (\approx 0.09pu)$. This work employs $L_{arm} = 0.15pu$, which meets the previous criteria and reduces the harmonics in circulating current. Thus, $L_{arm} = 10.82mH$.

E. Thermal model and lifetime

The junction temperature T_j and case temperature T_c of the semiconductor devices are important variables that directly affect the lifetime and the reliability. The methodology employed is based on a look-up table of losses obtained from the power modules datasheets. The thermal model employed is presented in Figure 4 [14].

Generally, the junction-to-case thermal impedance Z_{j-c} and the case-to-heatsink thermal impedance Z_{c-h} are obtained from the datasheets. The heatsink-to-ambient thermal impedance Z_{h-a} presents a larger capacitance when compared to power module which is generally disregarded in thermal simulations. Additionally, the thermal resistance can be approximated by:
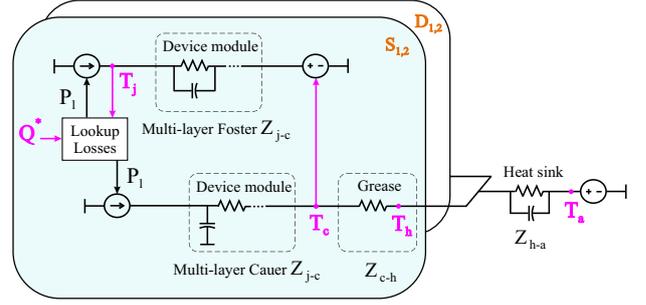
Fig. 4. : Thermal model of the power devices in the half-bridge SM with a common heatsink.

$$R_{h-a} = 6N\frac{T_{h,max} - T_a}{P_{lt}}, \tag{28}$$

where P_{lt}, $T_{h,max}$ and T_a are the total power losses of the converter, maximum heatsink temperature and ambient temperature, respectively. Considering $T_a = 40\,^{\circ}$C, $T_{h,max} = 80\,^{\circ}$C and P_{lt} as 0.5 % of rated power in the worst case, $R_{h-a} = 0.12K/W$ is obtained.

The lifetime of power modules is strongly related with the thermal cycling, that causes cyclic thermo-mechanical stress in all components and joints, finally leading the device to fail. In applications with critical mission profile, the lifetime evaluation is strongly recommended. The lifetime analysis is based on the flowchart of Figure 5. Firstly, the power losses are estimated for the mission profile. The lifetime consumption (LC) is dependent on the average temperature T_m, the cycle amplitude ΔT_m and the heating time t_{on}. Furthermore, the lifetime models consider constant values for T_m, ΔT_m and t_{on}. Therefore, a rainflow counting method is employed [3] in order to identify the characteristics of each cycle.
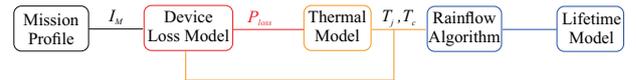
Fig. 5. : Devices lifetime flowchart.

The lifetime model employed in this work is the model provided by ABB for Hi-Pak power modules [15], based on the number of cycles to failure N_f. This model employs the junction and case temperatures of the devices and returns the lifetime consumption of the bond wire, chip solder and base plate. Considering this same profile for one year, N_f is calculated for one cycle and multiplied by the total in one year to obtain the accumulated damage, using the Palmgren-Miner rule [16]. The B_{10} approach considers a probability of 10% failure of the power module and is employed in this work. Finally, the lifetime in years is the inverse of the annual damage.

III. Case Study

The main circuit parameters of the designed DSCC-MMC STATCOM are presented in Table I. For the validation of the control developed in this work, 1 pu of positive sequence reactive power is injected in the grid by the converter until $t = 0.1s$. After, the STATCOM is commanded to inject 1

pu of negative sequence reactive power. The simulations were performed in *softwares PLECS* and *MATLAB*, aiming to validate the proposed design methodology and to estimate the lifetimes.

TABLE I: Parameters of the modular multilevel converter.

Parameter	Value
Grid voltage (v_g)	13.8 kV
Line frequency (f_n)	60 Hz
pole to pole dc voltage (V_{dc})	28 kV
Rated power (S_n)	7 MVA
Transformer inductance (L_g)	2.89 $mH(0.04pu)$
Transformer X/R ratio	18
Arm inductance (L_{arm})	10.82 $mH(0.15pu)$
Arm resistance (R_{arm})	0.14 $\Omega(0.005pu)$
SM capacitance (C)	2 mF
Nominal SM voltage ($v_{sm,n}^*$)	1.65 kV
Carrier frequency (f_c)	210 Hz
Number of SMs (N)	17 per arm

Two part numbers are analyzed in this work: 5SNG 0250P330305 (Solution 1 - 250 A) and 5SND 0500N330300 (Solution 2 - 500 A), both from ABB. The lifetime, energy losses and cost of each solution are compared. The mission profile is based on a reactive power measurements obtained from the factory, according to Figure 6. The data were collected during one week with a sample time of 5 min.
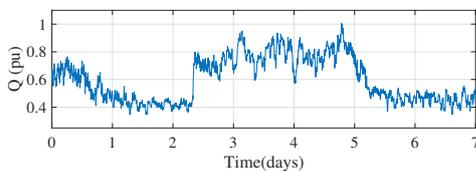
Fig. 6. : Mission profile from the factory.

IV. Results

The instantaneous active and reactive power injected in the grid are illustrated in Figure 7. As observed, at $t = 0.1s$ the converter injects 1 pu of negative sequence current. Thereby, the powers present oscillatory components at the doubled line frequency (120 Hz). The instantaneous active power presents an average value that supplies the power losses of the converter.
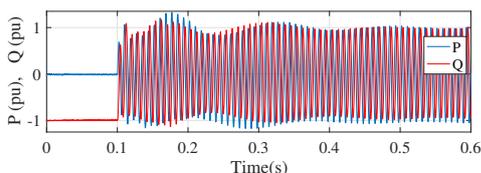
Fig. 7. : Instantaneous active and reactive power injected by the DSCC-MMC STATCOM.

In terms of grid current, when 1 pu of positive sequence reactive power is injected by the converter, the currents are balanced as observed in Figure 8. However, considering 1 pu

of negative sequence reactive power, the currents are slightly unbalanced since an amount of positive sequence active power is necessary to supply the losses.
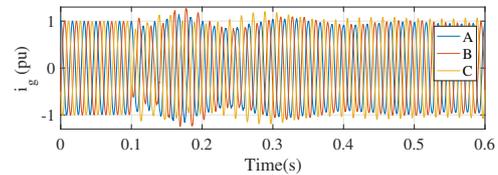
Fig. 8. : Grid currents injected by the DSCC-MMC STATCOM.

Figure 9 (a),(b),(c) shows SM capacitor voltages at the upper arms. The voltage ripple depends on the values of positive and negative sequences. With 1 pu negative sequence a different ripple can be observed for each phase due to the imbalance shown in Figure 8 .The designed capacitance value guarantees that the maximum ripple in steady-state for the most stressed phase is within the 10 % range, which is evidenced by dashed lines. Figure 9 (d), shows the overall average capacitor voltage. Finally, it can be seen that the SM voltages are well balanced and controlled. The disturbance in capacitor voltages is rejected in 350 ms.
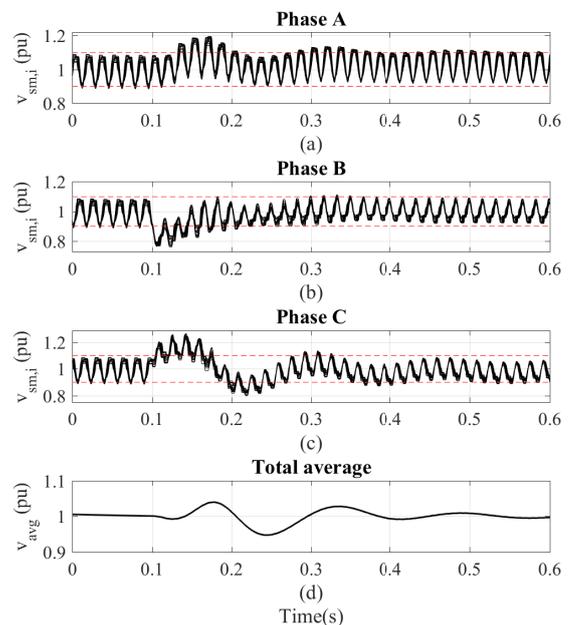
Fig. 9. : SM voltages: (a) Upper arm of phase A; (b) Upper arm of phase B; (c) Upper arm of phase C; (d) Total average.

Considering the mission profile, the thermal stresses in the power devices are illustrated by the Figures 10 (a) and (b). As observed, the 500 A power module presents smaller temperatures in semiconductors when compared to the 250 A power module. The switches D1 and D2 are more stressed than S1 and S2 for the profile, since reactive power is processed.

Using the temperature profile of the devices, the lifetime consumption at the different components of the power mod-
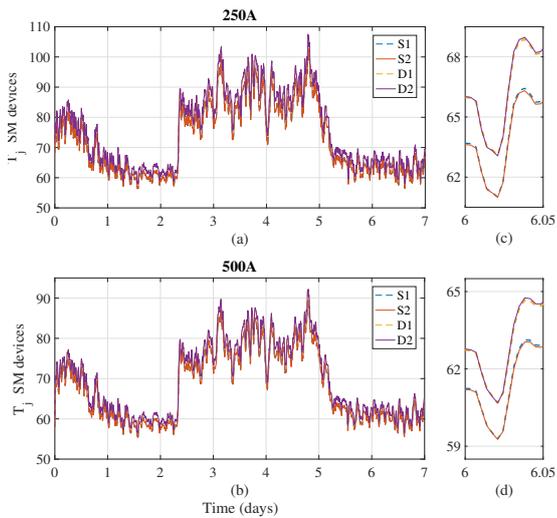
Fig. 10. : Junction temperatures of the devices in a SM for two IGBT solutions: (a) 250A; (b) 500A.

ule can be obtained. This result is shown in the Fig. 11. As observed, the base plate is the most stressed part of the power module, followed by the chip solder and finally the wire bond. The increase in the power module current results in a considerable increase in the lifetime of the converter, since the thermal stress is strongly reduced.
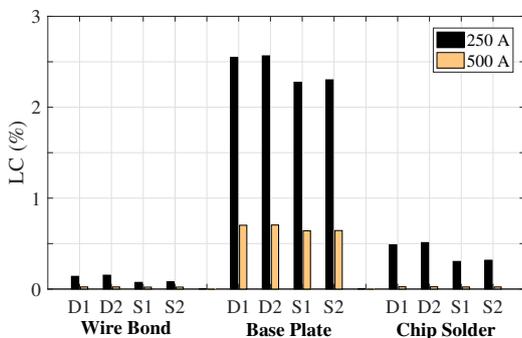
Fig. 11. : Lifetime consumption (%) of the two IGBT solutions.

Finally, Table II presents the comparison of the two IGBT solutions employed in this work in terms of lifetime, energy losses and cost. The values are in per unit (pu) in the base of the smaller current solution. Only the base plate lifetime consumption of the most stressed device D2 is considered for lifetime comparison. The cost was evaluated based on market data. As observed the larger current solution presents a increase in the lifetime of 3.6 times and almost 5 % less losses, however, the cost of the power modules is increased in 60 %.

TABLE II: Comparison of the IGBT solutions.

Solution	Lifetime (pu)	Energy losses (pu)	Cost (pu)
250 A	1	1	1
500 A	3.6	0.956	1.6

V. Conclusions

This work presented a design methodology of the main circuit parameters of DSCC-MMC considering both positive and negative sequence current compensations. The dc-link voltage, number of SM, semiconductor devices, SM capacitance and arm inductance were designed for a 7 MVA STATCOM. The simulation results validate the proposed design and control methodology for the converter.

Furthermore, a detailed study of power modules lifetime based on a DSCC-MMC STATCOM was presented. A real mission profile of a factory is considered. During reactive power compensation the diodes of each SM are the most stressed devices. Two IGBTs with different current ratings were compared. As observed, the base plate of power modules was the most stressed part of the design, since only long term analysis was implemented.

The solution based on 500 A power modules presents significant improvements in terms of energy losses and lifetime. However, this solution presents a larger cost. Furthermore, it is important to mention that the final cost of the converter will not be 60 % larger than the first solution, since the power modules represent a fraction of the final cost of the MMC STATCOM. Additionally, the energy losses of the first solution are larger and its operation presents a larger cost.

VI. Acknowledgments

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