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High Level Performance Models of Double-Star MMC Converters

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***Abstract*— The development of Modular Multilevel Converter (MMC) technology is a breakthrough in the field of High and Medium Voltage applications. In general, simulations are needed to study a new application and to analyze the impact of a new converter in power systems. Thus, accurate models able to represent the dynamics present in the converter are required. This work aims to compare two MMC average models and one average model with three modulation strategies in order to propose high level models, able to represent the MMC dynamics, such as the injected active and reactive power, and the SMs capacitor voltages, without the necessity of switching models. A case study is presented considering a Double Star (DS) MMC, connected in a distribution system during an unbalanced voltage sag. The results shows that considering MMC average models only the steady state can be represented. On the other hand, when the modulation techniques are considered together with the MMC average models, it is possible to represent the capacitor voltage ripples and the grid current ripples increasing slightly the necessary processing time.**

I. INTRODUCTION

Among the voltage source converter (VSC) technologies used in distribution and high-voltage direct current (HVDC) systems, modular multilevel converter (MMC) has important improvements compared to traditional two-level (2L) VSC. Among the advantages of MMC the most important ones are a very low harmonic voltage content and low switching losses [1]. The lower harmonic content allows the elimination of tuned filters which are mandatory in a 2L-VSC [2].

Detailed models used to simulate MMC topology can include the representation of thousands of semiconductor switches. These models require small integration time steps, in order to accurately represent the switching events [3]. As a result the large number of IGBTs, diodes and capacitors create a computational challenge, related to total simulation time [3,4,6].

In power system studies, it is necessary to choose a model able to represent the desired phenomenon with accuracy, avoiding unreasonably long simulation times [8]. MMC simulation models can be designed with different degrees of detail [7]. In this sense, the programmer or designer should be able to define clearly the simulation propose.

The goal of all simulations is to provide results in steady state and transient responses as close as possible to the real converter. This goal can be obtained based on complex models or simplified models. Several works presented in the literature show different models able to represent a MMC behavior [3-7]. In [5], a solution based on the Kirchhoff's Voltage and Current Laws is proposed, where, a large-scale system is divided in small-scale matrices, which are mathematically solved with the nodal analysis method. An accelerated model is obtained with a very high level accuracy model.

Other works present solutions based on average-value model (AVM) [3,6,7]. These simplified models have the purpose to replicate the average response of switching devices, converters, and controls by using time average functions and controlled current and voltage sources [3]. The average value models approximate system dynamics by neglecting switching events, requiring less computational resources and larger integration time steps [6].

In this work, the performance of two MMC averaged models is evaluated considering three different modulation strategies. The MMC average models are able to represent the arm and SMs voltages through mathematical equations, approximating the system dynamics by neglecting the switching details. The association of MMC average models with modulation strategies insert the SMs switching dynamic. In this work three traditional modulation strategies are analyzed, i.e. phase shift carrier (PSC), level-shift carrier (LSC) modulation and nearest level control (NLC). Associated with the modulation techniques two balancing methods are used, i.e. local balancing and sorting and selection (S&S) strategies.

The present work is organized as follows. In Section II, two MMC average models are described, and in Section III three modulation strategies are introduced. In Section IV a case study considering an unbalanced grid voltage in a distribution system is presented. Also the main parameters are shown. Section V shows the results comparing all five models and a comparison between these models is done in terms of computation time and dynamic behavior. Finally, in Section VI the main conclusions are stated.

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II. HIGH LEVEL PERFORMANCE MODELS

A. Leg-Level Averaged Model

The main feature of a Leg-Level Averaged (LLA) can be described in terms of the sum capacitor voltages in each arm. Assuming the same voltage distribution in all arm submodules (SMs), the upper and lower arm voltage, and the circulating [4] current, can be expressed by:

$$\frac{d}{dt}\begin{bmatrix} i_c \\ v_{cu}^{\Sigma} \\ v_{cl}^{\Sigma} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{n_u}{2L} & -\frac{n_l}{2L} \\ \frac{Nn_u}{C_{sm}} & 0 & 0 \\ \frac{Nn_l}{C_{sm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_c \\ v_{cu}^{\Sigma} \\ v_{cl}^{\Sigma} \end{bmatrix} + \frac{1}{2}\begin{bmatrix} \frac{v_d}{L} \\ \frac{Nn_u i_s}{C_{sm}} \\ -\frac{Nn_l i_s}{C_{sm}} \end{bmatrix}, \quad (1)$$

where i_c is the circulating current, i_s is the output current, v_{cu}^{Σ} and v_{cl}^{Σ} are the sum of the capacitor voltage in upper and lower arm, respectively, v_d is the pole-to-pole dc-bus voltage. R is the arm resistance, L is the arm inductance, C_{sm} is the SM capacitance, n_u and n_l are the insertion index in the upper and lower arm, respectively, and N is the number of submodules per arm.

LLA models can be used to create a complete simulation model including the output-current and circulating-current controllers, as well as arm-balancing control using direct voltage control [4]. Fig. 1 shows a LLA diagram that can be easily implemented in simulators that can represent Laplace transfer functions, where, v_u and v_l are the arm voltage.

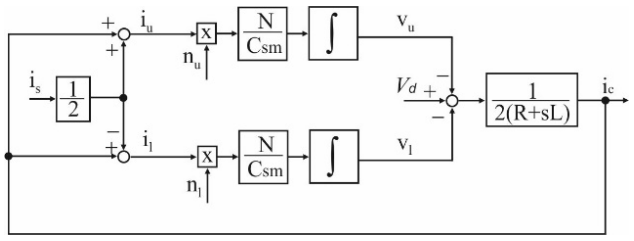

Figure 1. Leg Level Averaged (LLA) model.

The drawbacks of LLA models are the inability to represent PWM dynamics and also the SM capacitor voltage .

B. Submodule Level Averaged Model

In order to increase the details presented in LLA model, equation (1) can be used to split the arm voltage in SM voltages, creating a Submodule Level Averaged (SLA) model, as given by:

$$\frac{d}{dt}\begin{bmatrix} i_c \\ v_{cu,i} \\ v_{cl,i} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{n_{u,i}}{2L} & -\frac{n_{l,i}}{2L} \\ \frac{Nn_{u,i}}{C_{u,i}} & 0 & 0 \\ \frac{Nn_{l,i}}{C_{l,i}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_c \\ v_{cu,i} \\ v_{cl,i} \end{bmatrix} + \frac{1}{2}\begin{bmatrix} \frac{v_d}{L} \\ \frac{Nn_{u,i} i_s}{C_{u,i}} \\ -\frac{Nn_{l,i} i_s}{C_{l,i}} \end{bmatrix}, \quad (2)$$

where $v_{cu,i}$ and $v_{cl,i}$ are the voltage in the SM i of upper and lower arm respectively; $n_{u,i}$ and $n_{l,i}$ can take values of 0 (bypass a SM) or 1 (insert a SM), and are defined as the insertion index of the SM i of the upper and lower arm, respectively; $C_{u,i}$ and $C_{l,i}$ are the capacitance of the SM i in the upper and lower arm, respectively.

Thus, it is possible to vectorize the model for N SMs, as shown in Fig. 2. $G_{u,i}$ and $G_{l,i}$ are vectors composed of zeros and ones, indicating if the SM should be inserted or bypassed.

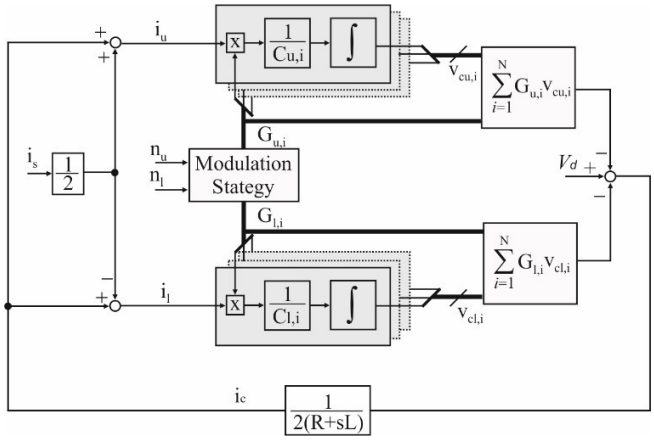

Figure 2. Vectorized diagram of Submodule Level Averaged (SLA) model.

Fig. 3 shows a complete structure that can be easily implemented in simulation software. The output-current control, using a proportional-resonant controller PR, a circulating-current controller, using a second resonant controller PR_2 and also a droop control, represented by the gain R are included. Also, the arm-balancing control is highlighted. The grid voltage is given by v_α, and a low-pass filter (LPF) and a delay transfer function (TF) are also necessary.

The drawbacks of SLA models are the inability to represent PWM dynamics and also capacitor voltage unbalance within the arm [4].

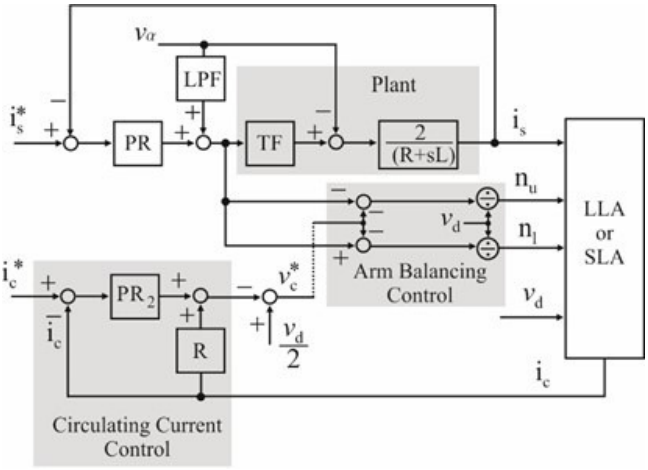

Figure 3. Complete model considering control structure.

III. MODULATION STRATEGIES

A. *Phase Shift Carrier and Local Balancing Strategy*

The PSC modulation method is one of the most commonly used modulation strategy for MMCs when low number of SM is present [9]. In this modulation strategy, each SM in the arm has its own carrier wave, which is phase shifted from the other SM carriers, as shown in Figure 4.

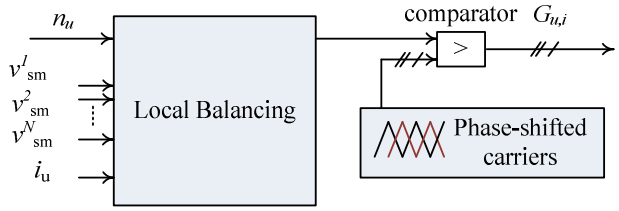

Figure 4. Schematic diagram for phase shift carrier modulation strategy.

B. *Level Shift Carrier and Sorting and Selection Balancing Strategy*

A variation of PSC strategy is known as Level Shift Carrier (LSC). In this modulation strategy the carriers waves instead of phase shifted they are shifted vertically. In order to ensure the capacitor voltage balance, LSC strategy requires an additional strategy to balance the SM capacitor voltages. The algorithm called sorting and selection (S&S), can properly select the SM in the arm to be inserted or bypassed.

Basically, the SM capacitor voltage is measured and sorted. Then, during a positive arm current, the SM with the lowest voltage will be selected to be inserted and charged, while the SM with high voltage will be bypassed. During a negative arm current respectively, the SM with the highest voltage will be selected to be inserted to get discharged, while the SM with low voltages are bypassed. Figure 5 shows the modulation strategy considering LSC and S&S algorithm.

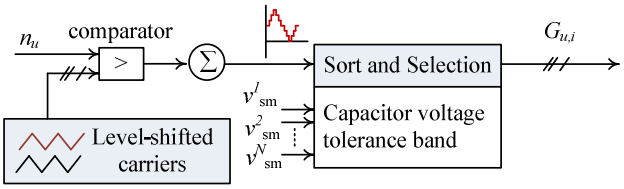

Figure 5. Schematic diagram of level shift modulation strategy.

C. *Nearest Level Control and Sorting and Selection Balancing Strategy*

The concept of NLC strategy is to determine the nearest voltage level in each sampling period from the reference output voltage. In order to perform this task, the insertion index n_u is first obtained and scaled with the number of SM in the arm N, at each sampling period, as shown in Figure 6.

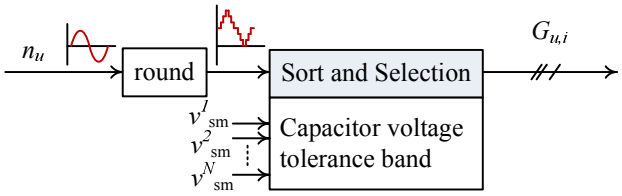

Figure 6. Control scheme of NLC strategy.

IV. CASE STUDY

To evaluate and compare the different models presented in the previous Sections, a double-star three-phase MMC converter, as shown in Fig. 7, is simulated in Matlab/Simulink. Basically, each phase of the MMC consists of 20 SMs connected in series defining an arm structure. The three legs of the MMC are then connected to the common dc-link capacitor C_{dc}. Each SM consists of a half-bridge power module and a SM capacitor C_{sm}. An arm inductor L and its internal resistance R are used to suppress the high frequency components in the output voltage caused by the SMs switching.

The system parameters are shown in Table 1. The MMC design considers a maximum ripple in the SM capacitor voltage of 10%. A case study is performed considering an unbalanced voltage sag in a distribution system, starting at 0.3 s, with a duration of 0.4s, as shown in Figure 8.

All combinations between MMC models and modulation strategies are shown in Table 2. Models 1 does not require a modulation strategy. Model 2 uses a SLA MMC model without a modulation strategy and all SMs are considered with the same insertion index. Models 3-5 use the SLA model combined with each of the modulation techniques presented in Section III.

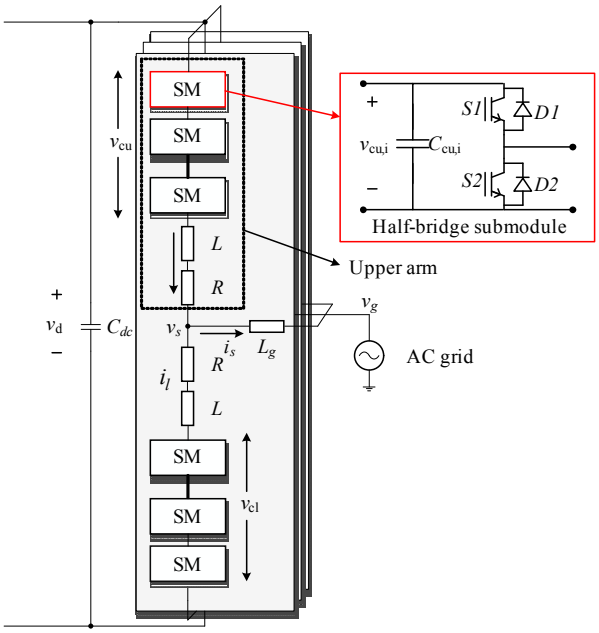

Figure 7. DS-MMC system configuration.

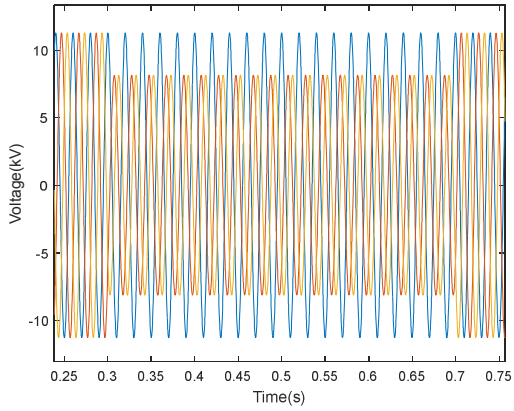

Figure 8. Voltage sag profile (V_g) used to compare all models.

Table 1: System Parameters of the DS-MMC.

Variable	Description	Value
N	Number of SM per arm	20
C_{sm}	SM capacitance (mF)	5.1
C_{dc}	dc-link capacitance (mF)	0.24
L	Arm inductor (mH)	4.7
L_g	Grid-side inductor (mH)	0.5
S	Rated power (MVA)	15
V_{SM}	Sub-module voltage (kV)	2.5
f	Grid frequency (Hz)	50
v_g	Grid voltage (kV)	13.8
v_d	Dc-link voltage (kV)	50

Table 2: Case studies considering MMC models and the modulation strategies.

	MMC Model	Modulation	Frequency (Hz)
Model 1	LLA	-	-
Model 2	SLA	-	-
Model 3	SLA	PSC and Local Balancing	333
Model 4	SLA	LSC and S&S	333*N
Model 5	SLA	NLC and S&S	-

V. RESULTS

The first variable analyzed is the circulating current. In a double-star MMC topology, each phase has its own circulating current, as shown in Figure 9. For both models 1 and 2 that do not consider a modulation strategy, no ripple can be simulated on the circulating current. On the other hand, models 3, 4 and 5 present ripples around 15% in the circulating current.

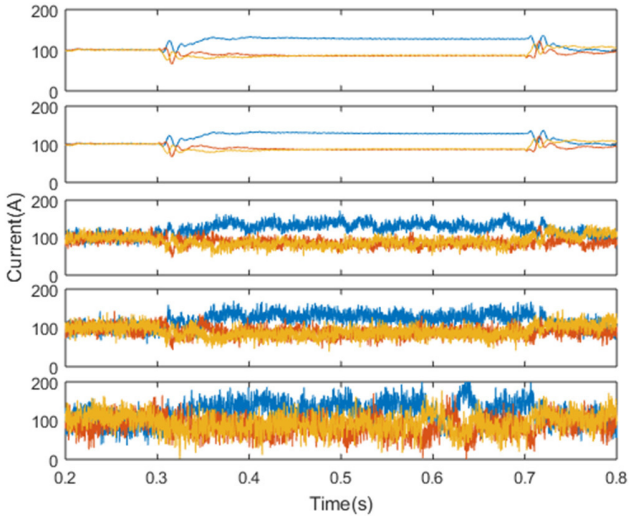

Figure 9. Circulating current from Model 1, Model 2, Model 3, Model 4 and Model 5, respectively, from top to down.

Considering the active power injected into the ac-grid, during the pre-fault condition, the DS-MMC is injecting 1 p.u. of active power, as shown in Figure10. During the unbalanced voltage sag, there are negative sequence components in the ac-grid voltage, producing oscillations in the injected active power. A similar behavior is observed in the injected reactive power, as shown in Figure 11. In fact, the models can be divided into two groups with their main difference being the simulated ripple, i.e. models 1 and 2 form the first group, while models 3-5 form a second group. Between the models of the same group, little difference can be observed in the obtained results.

The SM capacitor voltages are the most affected by the chosen model. Model 1 cannot represent the SM capacitor voltage, thus, only the arm voltage is observed. Even during the unbalanced voltage sag, the arm voltage keeps inside the designed range of 10%.

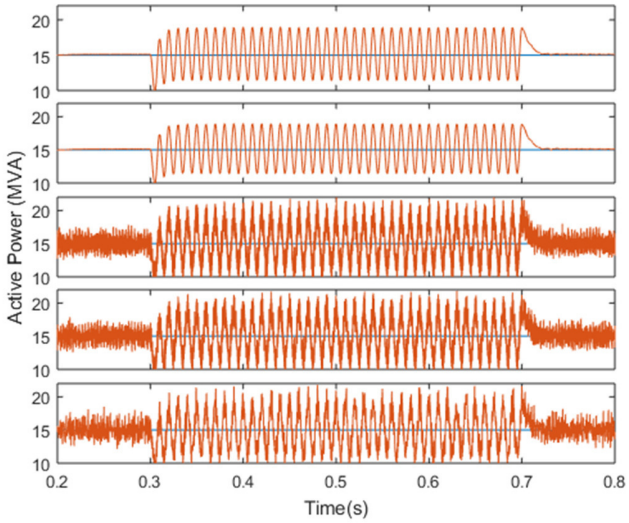

Figure 10. Injected active power into the grid from Model 1, Model 2, Model 3, Model 4 and Model 5, respectively, from top to down.

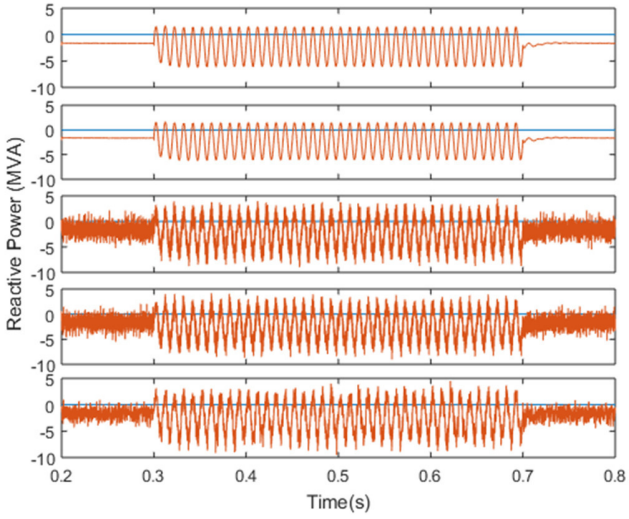

Figure 11. Injected reactive power into the grid from Model 1, Model 2, Model 3, Model 4 and Model 5, respectively, from top to down.

In model 2 several SMs capacitor voltages operate outside the tolerance band. This drawback is not observed in models 3, 4 and 5, once the modulation strategy can bring the SM capacitor voltages to operate inside the SM voltage tolerance band. Model 4, using SLA representation and LSC+S&S strategy presents the best regulation of SM capacitor voltages.

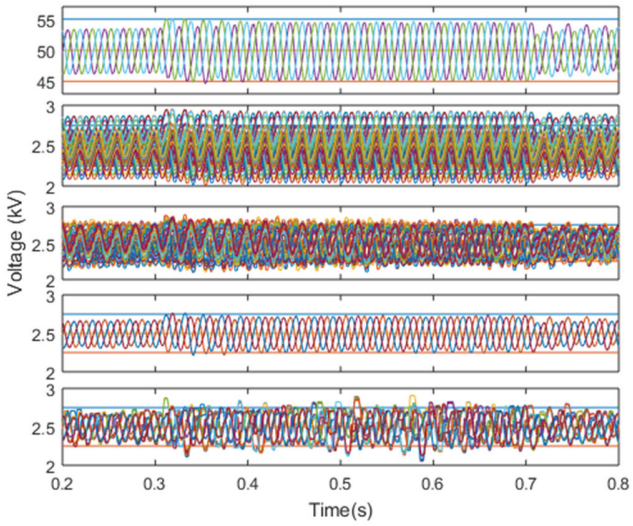

Figure 12. Arm voltage for Model 1 and SM capacitor voltages for Model 2, Model 3, Model 4 and Model 5, respectively, from top to down.

Finally, the computer processing time is evaluated, considering simulations with different numbers of SMs. Model 1 is the base case scenario, once this model does not represent the SM capacitor voltage and its processing time is constant, even when the number of SM increase.

Model 2 needs low processing time, although, it is affected by the number of SMs. Considering 400 SMs per arm (2.400 SMs in total), model 2 needs 14.8 seconds to perform a simulation of 1 second, as shown in Fig. 13.

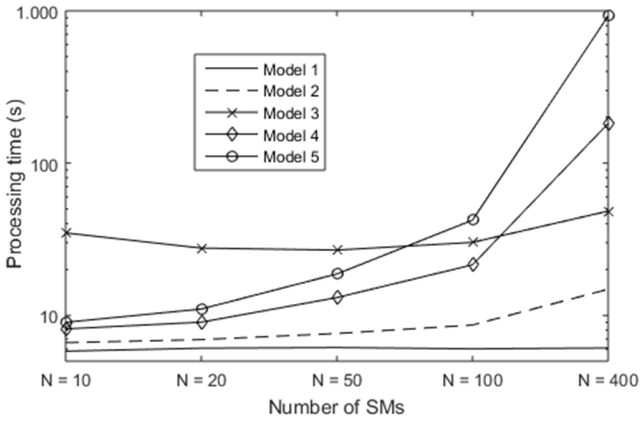

Figure 13. Computer processing time during a voltage sag simulation (simulation time = 1 s, using a multicore PC with an Intel Core i7-4500 1.8-GHz CPU and 8.0 GB RAM).

Model 3 presents an interesting behavior. Considering few SMs, for example 10 SMs per arm, its processing time is around 34.7 seconds, the higher processing time of all models. All simulations were implemented using variable step size and the solver method ODE45.

In model 3 is observed that when the number of SMs is very small, for example N = 10, the simulation step size is reduced compared with N = 50. Thus, even increasing the number of SM, the simulation time decrease. When the number of SM is higher than 50, the increase in the simulation step size is not more observed. Considering 400 SMs per arm, the processing time is 48 seconds, as shown in Fig. 13, a value very small compared with models 4 and 5.

Models 4 and 5 use a sorting and selection algorithm. To sort all SMs, it is necessary to compare the SM capacitor voltage creating an ordered list. In these models the number of SMs strongly affect the processing time. Considering 400 SMs per arm, models 4 and 5 require 181 and 924 seconds to perform a simulation of 1 second, respectively.

To simulate models 3 and 4 are necessary carrier waves. In model 3 the frequency from the carrier waves was kept constant and equal to 333Hz. However, these waves need to be phase shifted, affecting directly the processing time.

On the other hand, in model 4 the frequency from the modulation carries are not phase shifted, decreasing the simulation step size. However, in model 4, the frequency from the carrier waves is proportional with the number of SMs. Thus, when the number of SMs increase, the processing time also increase.

VI. CONCLUSIONS

This work presented a combination of average models and the most used modulation strategies, in order to obtain high performance models, able to represent the mains characteristics of a DS-MMC.

The SM capacitor voltages are influenced by the modulation strategies, and the results are affected by the model choice. However, the grid variables, such as active and reactive power, and the grid current present similar behavior for all studied models.

Moreover, a comparison of the models shows that it is possible to include a modulation strategy, making the models more accurate, without affecting significantly the processing time, as shown in model 3. On the other hand, modes using sorting algorithm do not have a good time performance when the number of SMs increase.

In fact, depending on the aim of the study, it is recommended that if the inner dynamics of the MMC are not the focus, the LLA model can be used to simulate the interaction of the converter with the connected power system. However, in cases where the MMC dynamics and its internal balancing are considered important, the SLA model with a modulation technique should be preferred.

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