GESEP – Gerência de Especialistas em Sistemas Elétricos de Potência

Título:

An improved solar array simulator topology based on LCL filter

Autores:

S. P. Freitas, N. A. C. Fernandes, V. F. Mendes, A. F. Cupertino and H. A. Pereira.

Publicado em:

8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

Data da publicação:

2017

Citação para a versão publicada:

S. P. Freitas, N. A. C. Fernandes, V. F. Mendes, A. F. Cupertino and H. A. Pereira, "An improved solar array simulator topology based on LCL filter," 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, 2017, pp. 1-7.

An Improved Solar Array Simulator Topology Based on LCL Filter

Shirleny P. Freitas[1], Natália A. C. Fernandes[1], Victor F. Mendes[2], Allan F. Cupertino[1,2] and Heverton A. Pereira[1,3]

[1] Electrical Engineering Postgraduate Program
CEFET-MG – UFSJ, Minas Gerais, Brazil
Av. Amazonas 5253, 30421-169, Belo Horizonte, Brazil
shirlenypfreitas@gmail.com, nattthyfernands@gmail.com,
allan@des.cefetmg.br

[2] Graduate Program in Electrical Engineering
Federal University of Minas Gerais
Av. Antônio Carlos 6627, 31270-901, Belo Horizonte, MG, Brazil
victormendes@cpdee.ufmg.br

[3] Department of Electrical Engineering
Federal University of Viçosa
Av. P. H. Rolfs s/nº, 36570-000, Viçosa, MG, Brazil
heverton.pereira@ufv.br

***Abstract*— Photovoltaic energy has gained prominence in the current context of energy generation. The fundamental element of a photovoltaic system connected to the electric grid is the electronic converter. In order to be marketed, electronic converters must be tested and certified in accordance with current standards. In the certification process, an equipment known as a solar array simulator (SAS) is used. This work presents the modeling and the control structure of a 10 kW SAS for tests of electronic converters for photovoltaic systems. The novelty introduced in this work is the insertion of a passive filter at the SAS output. The purpose of this filter is to reduce the output current ripple, which is directly influenced by the input capacitance of the inverter under test (uncertain variable). It is considered a structure with 2 stages that allows a greater flexibility in relation to the arrangements to be emulated. The results showed that with the use of a passive filter the topology presented operational advantages being able to represent the characteristics of the photovoltaic arrangement and a considerable reduction in the output current ripple of the simulator.**

Keywords*— Solar array simulator, Control of dc/dc Converters, Photovoltaic Solar Energy.

I. INTRODUCTION

The fundamental element of a grid-photovoltaic system is the electronic converter. This component is responsible for the integration between the photovoltaic panels and the power grid. In order to be commercialized, photovoltaic inverters must be certified. Generally, the tests require the use of an equipment called solar array simulator (SAS). [1] [2]

The calculation of the current reference can be complex due to the non-linear behavior of the solar panel. Several methods are presented in the literature, such as the analog method [3], the method of the tables [4], the analytical method [5], the hybrid method [6] and methods based on artificial neural networks [7] [8].

Results presented by [9] illustrates the use of a three-phase voltage source PWM rectifiers as a solar array simulator. However, the dc-link voltage obtained has a minimum value, which guarantees the correct operation of the rectifier. Thus, the minimum direct voltage obtained is equal to the utility line voltage peak. To overcome this problem, a transformer needs to be employed in order to reduce the ac voltage and consequently, the direct voltage obtained.

In view of this problem, a flexible SAS is presented in [1]. The topology is based on a three-phase PWM rectifier in cascade with a dc/dc bidirectional buck converter, as illustrated in Fig. 1. A problem reported in this topology is the high output current ripple when the SAS is employed in the test of inverters with high dc-link capacitance.

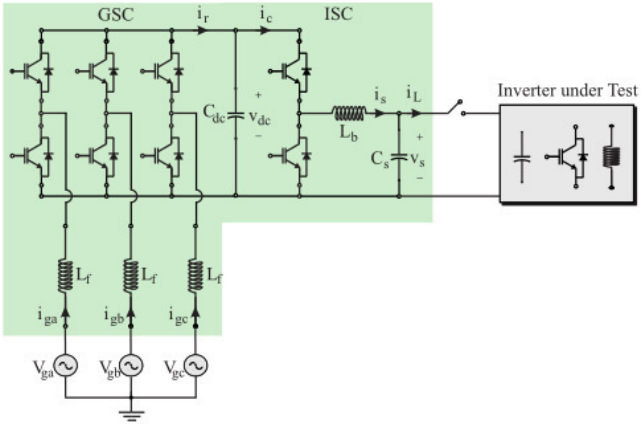


Fig. 1. Structure of solar array simulator proposed by [1] .

Considering this problem, this work presents a solution based on the insertion of an inductance at the SAS output, as illustrated in Fig. 2, in order to obtain a reduction in the ripple of SAS output current. The design methodology of the passive components is analyzed and a comparisons in terms of dynamic behavior and output current ripple are presented. The proposed

978-1-5090-5339-1/17/$31.00 ©2017 IEEE

topology is designed for the testing of 10 kW single-phase and three-phase photovoltaic inverters.

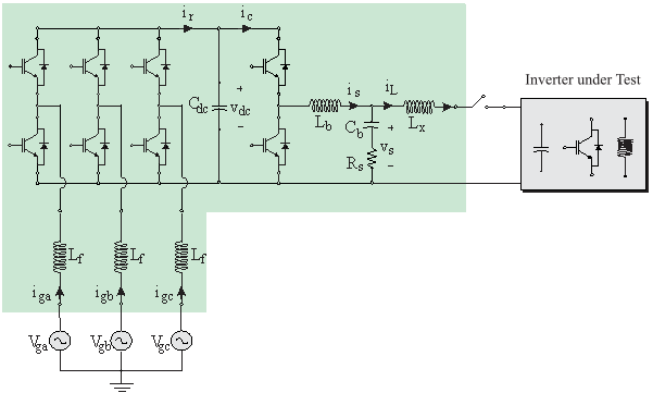


Fig. 2. Proposed structure of solar array simulator.

II. MODELING OF THE SOLAR ARRAY SIMULATOR

A. Ac/dc stage

The SAS rectifier stage is based on a three-phase PWM converter. An inductive filter is used in order to reduce the harmonic content generated by the IGBTs switching. The design of this filter is presented in [10]. The classical control structure based on synchronous reference frame (dq) was employed to control the PWM rectifier. For the system modeling, grid voltages are considered balanced and without harmonic components. In this situation, the differential equations in the synchronous reference frame dq are written as:

$$\begin{cases} v_d = -R_f i_d - L_f \dfrac{di_d}{dt} + \omega_n L_f i_q + v_{gd} \\ v_q = -R_f i_q - L_f \dfrac{di_q}{dt} - \omega_n L_f i_d + v_{gd} \end{cases} \quad (1)$$

where v_{gd}e v_{gq} are the direct and quadrature components of grid voltage, v_d and v_q are the components of the fundamental voltage generated by the rectifier, i_d and i_q are the components of the grid currents, L_f is the filter inductance and R_f is the filter resistance.

Synchronization of the converter with grid voltage is based on a Dual Second Order Generalized Integrator Phase-Locked Loop (DSOGI-PLL), proposed by [11]. This PLL has good responses for voltage unbalances and voltage harmonics. The modulation strategy implemented is the space vector PWM (SVPWM) technique.

The control structure consists in two cascade loops: internal loops controlling the direct and quadrature components of the grid currents and external loops regulate the dc bus voltage and the reactive power injected into the grid [12]. The control structure of PWM rectifier is presented in Fig. 3. The terms $wLi_{gd} + V_d$ and wLi_{gq} are feedforward terms. The controllers are adjusted according to the methodology presented in [1].

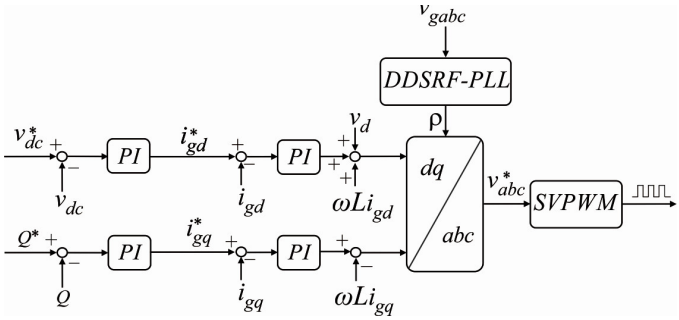


Fig. 3. Complete Control structure of PWM rectifier.

B. Dc/dc stage

The SAS proposed presents two operational modes, as suggested in Fig. 4.

- *Open-circuit control mode.* It is responsible for controlling the output voltage of the SAS when it is unloaded. In this situation, a reference voltage is the open circuit voltage of the emulated solar array;
- *Solar array simulator control mode*. Based on the voltage imposed by the converter under the test, the current reference is obtained based on the look-up table from I-V curve.

In this block diagram is possible to see both operation modes: the open-circuit control mode is based on a proportional-integral (PI) compensator. The SAS control mode is based on a lookup table of I x V curves. This method consists in the following steps: for a given value of solar irradiance G and temperature T_c, a table with the values of an I-V curve is chosen. The value of the output voltage is interpolated in this table and the result is the reference value of the inductor current. This interpolation is dynamic [4].

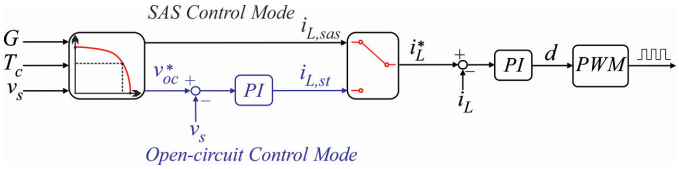


Fig. 4. Complete control structure of dc/dc converter.

In the dc/dc converter modeling, the following points were considered:

- The converter switches are driven in complementary;
- The dc bus voltage of the rectifier is constant;
- Only the ohmic losses in the inductor of the converter are considered.

Assuming these simplifications, consider the equivalent circuit of the cc/cc stage to perform the simulation results, is shown in Fig. 5.

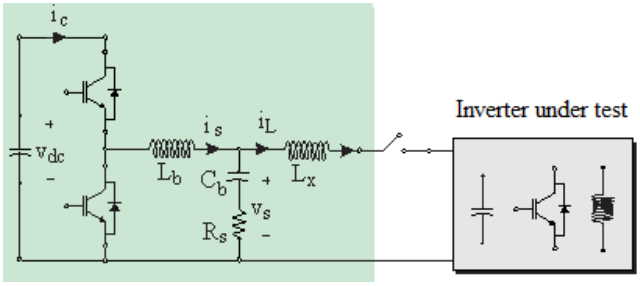


Fig. 5. Panel emulator stage cc / cc model.

The current controller is used in both control modes of the SAS using PI controller. The adjustment of the controllers is performed according to the methodology proposed by [1]. A PI controller is also used in the voltage regulation circuit and adjusted by the pole allocation method.

The proportional and integral gains of the current loop are given by:

$$\begin{cases} k_{p,iL} = \dfrac{2\pi f_{c1}(L_b + L_x)}{V_{eb}}, \\ k_{i,iL} = \dfrac{2\pi f_{c1}(R_b + R_x)}{V_{eb}}, \end{cases} \tag{2}$$

where, f_{c_1} is the cut-off frequency of the current loop. Its value is limited to two decades below the converter switching frequency.

Similarly to the previous one, the proportional and integral gains of the voltage loop are given by:

$$\begin{cases} k_{p,v_s} = 2\pi(f_{c_2} + f_{c_3})C_b \\ k_{i,v_s} = 4\pi^2(f_{c_2} + f_{c_3})C_b \end{cases} \tag{3}$$

where, f_{c_2} and f_{c_3} are the frequencies of the poles of the closed loop. Typically these poles are separated from one another by a decade and the value of the largest of them must be allocated at least a decade below the cut-off frequency of the current loop. This is necessary to ensure proper operation of the cascade control.

The digital implementation of the control uses a sampling time equal to the switching frequency [13].

III. Inductance Design

At the SAS output, an inductor is inserted. Therefore, the SAS LCL filter can be interpreted as two cascade LC filters. The resonance frequency of the LCL circuit associated with the inverter under test capacitance C_{min} (in radians per second), is given by:

$$\omega_{res_1} = \sqrt{\frac{1}{L_X C_{min}}} \tag{4}$$

The equivalent frequency, measured in hertz, is:

In order to avoid resonance problems, this resonance frequency is allocated between 10 times the fundamental frequency and half of the switching frequency. Therefore,

$$\omega_{res_1} = \frac{2\pi f_{sb}}{3}. \tag{6}$$

Then, replacing (6) in (4) and isolating L_x, we have that the value of this inductance can be found taking into account the resonance frequency and the minimum capacitor value of the inverter in test, thus:

$$L_X = \frac{1}{\left(\frac{2\pi f_{sb}}{3}\right)^2 C_{min}}, \tag{7}$$

where f_{sb} is the switching frequency of the SAS. C_{min} is minimum value of the capacitance of the inverter under test. In this work this value was defined as 10 times smaller than the SAS output capacitor.

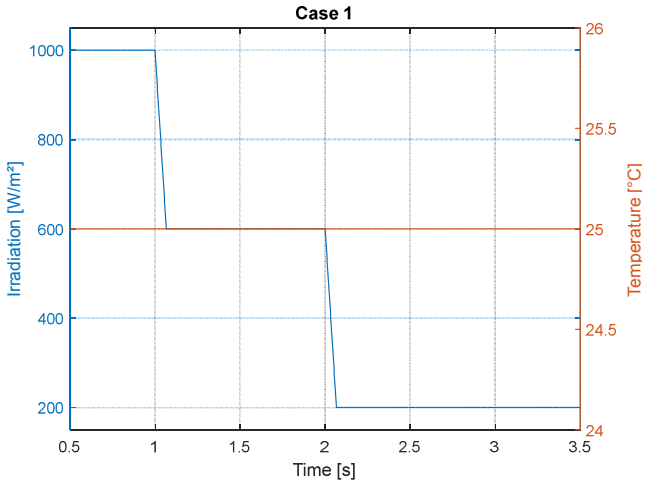
IV. Case Study

Two case studies are presented in order to validate the proposed structure. In the case study 1 presented in the Fig. 6 (a), the SAS is subjected to a profile irradiance variation, where initially the irradiance starts at 1000 W / m², falling to 600 W / m² and finally to 200 W / m², keeping its temperature at 25 ºC. In the second case study, the SAS emulates a variation in the PV temperature. Initially the temperature starts at 25 °C, increasing to 35 °C, keeping the irradiance at 1000 W / m², as shown in Fig. 6 (b).

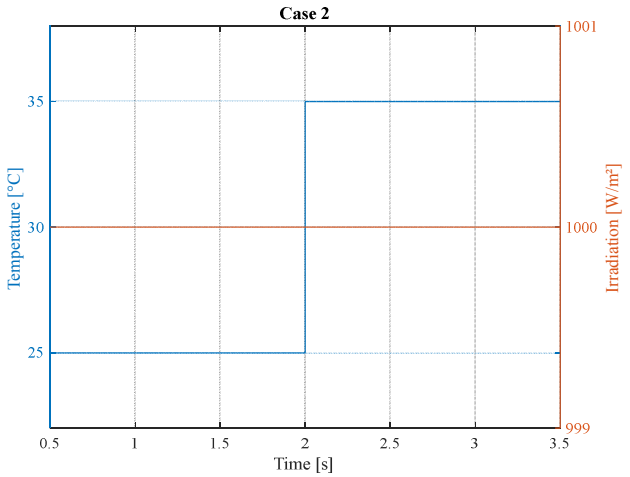
To validate the modeling, simulations were performed in Matlab/Simulink and PLECS. The system parameters are displayed in the TABLE I. and TABLE II. An arrangement with four strings in parallel with nine panels each one connected in series is simulated. Such arrangement results in an open circuit voltage of 337.5 V and a short-circuit current of 34 A in nominal conditions. The I-V curves of this arrangement is inserted into a look-up table, which is used in the SAS current control.

For the simulations, it was considered that the photovoltaic inverter under test can be represented by a boost converter, due to the fact that several topologies of photovoltaic inverters present a dc/dc stage dedicated to the maximum power tracking.

It is considered that the output dc-link of the boost converter behaves as a voltage source, for simplification. Fig. 7 shows the dc/dc boost converter and its control structure. The Perturb and Observe method (P&O) is employed to guarantee the maximum power point tracker [14]. The parameters of the simulated converter is presented in TABLE III.



(a)



(b)

Fig. 6. Case study. (a) Variation of irradiance and constant temperature. (b) Variation of temperature and constant irradiance.

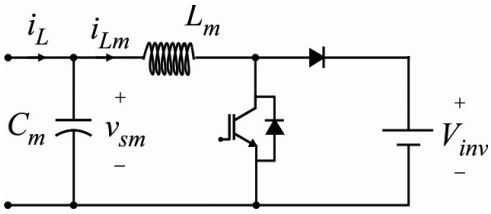
TABLE I. SOLAR PANEL DATA.

Parameters*	Value
V_{ocn}	37.5 V
I_{scn}	8.5 A
V_{mp}	31.29 V
I_{mp}	7.99 A
P_{max}	250 W
R_s	0.1739 Ω
R_p	379.0233 Ω
m	1
k_i	0.0043 A/K
k_v	-0.313 A/K

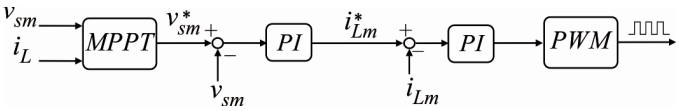
* (Provided for standard conditions: G_n = 1000 W/m^2, T_n = 25 °C).

TABLE II. PARAMETERS OF THE PHOTOVOLTAIC ARRANGEMENT EMULATOR.

Parameters	Symbol	Value
Nominal power	P_s	10 kW
Dc-link voltage	V_{dc}	430 V
Switching frequency	f_{sb}	30 kHz
Dc/dc stage inductance	L_b	2.3 mH
Dc/dc stage inductor Resistance	R_{lb}	0.021 Ω
Dc/dc stage capacitance	C_b	0.3 mF
Resonance resistor	R_s	1 Ω
Dc/dc stage output inductance	L_x	8.44 µH
Dc/dc stage output inductor Resistance	R_x	0.79 mΩ
Minimum value of the inverter input capacitance	C_{min}	30 µF
Proportional gain of current control	$k_{p,iL}$	0.051 Ω
Integral gain of current control	$k_{i,iL}$	177.95 Ω/s
Proportional gain of dc output voltage control	k_{p,v_s}	0.15Ω^{-1}
Integral gain of dc voltage control	k_{i,v_s}	6.66Ω^{-1}/s



(a)



(b)

Fig. 7. Converter boost MPPT: (a) Model considering simplification in the output dc bus; (b) Control structure used.

TABLE III. PARAMETERS OF THE BOOST CONVERTER UNDER TEST.

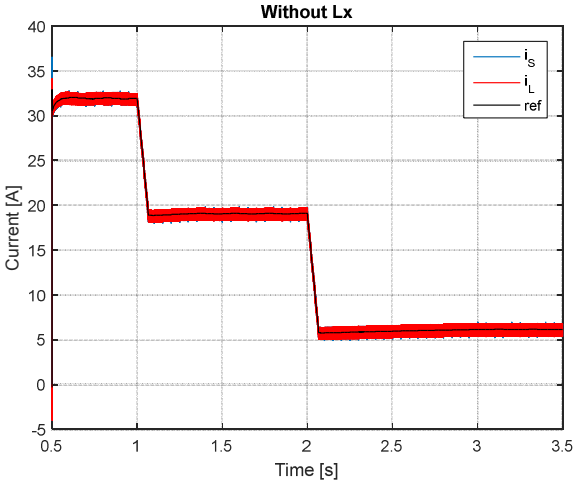
Parameters	Symbol	Value
Switching frequency	f_{sw}	15 kHz
Boost converter inductance	L_m	0.8 Ω
Boost converter Capacitance	C_m	3 mF
Inverter resistance	R_{lm}	0.01 Ω
Boost converter voltage	V_{inv}	420 V
Proportional gain of voltage control	$k_{p,v_{sm}}$	5.65 Ω^{-1}
Integral gain of voltage control	$k_{i,v_{sm}}$	220.46 Ω^{-1}/s
Proportional gain of current control	k_{p,iL_m}	0.017 Ω
Integral gain of current control	k_{i,iL_m}	0.219 Ω/s

V. SIMULATION RESULTS

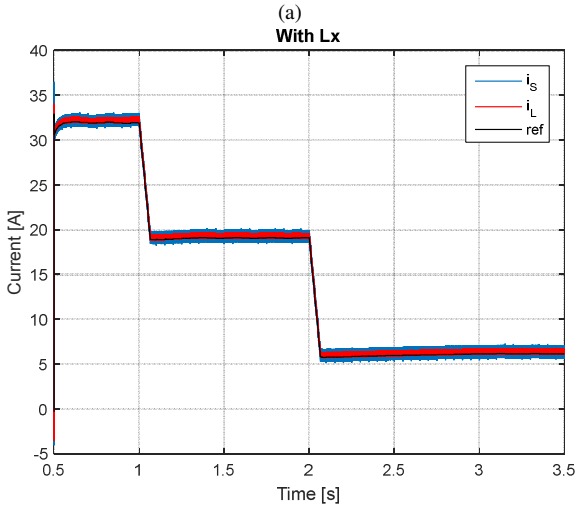
All results of the proposed SAS topology is compared with the SAS topology introduced by [1]. Fig. 8 presents the results when the SAS is submitted to a irradiance variation, as shown in case study 1. Fig. 8 (a) and (b) show the currents in the first inductance of the LCL filter (I_s) and in the second inductance (I_L). Although the dynamic behavior does not change, as shown in Fig. 8 (a), it is observed that the current I_s and I_L are practically the same and have a high ripple, while in Fig. 8 (b) the SAS output current ripple decreases considerably.

Fig. 8 (c) and (d) show the SAS output voltage and the SAS output power, respectively. When the second inductor is present, the MPPT dynamic from the inverter under test is few affected, providing a topology with smaller output ripple.

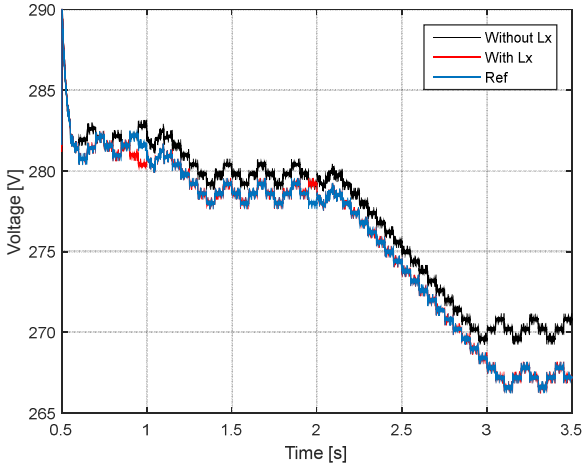
Fig. 9 shows the SAS dynamics for the cases with and without the second inductor in the plane P x V. It is observed that in terms of performance the transition is very similar, but in steady state, the topology where the second inductor is present follows the reference with small variations, having a better approximation to the point of maximum power.



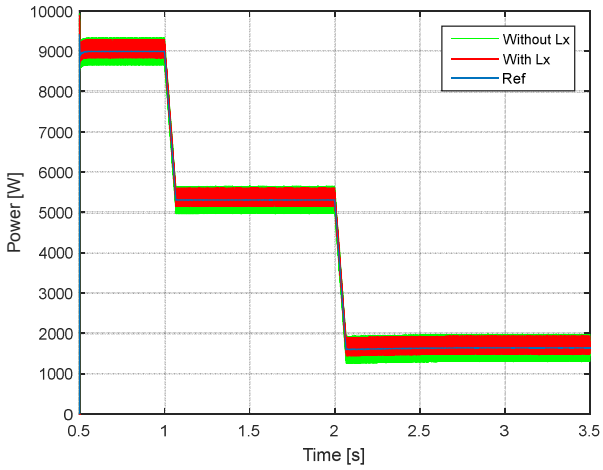
(a)



(b)



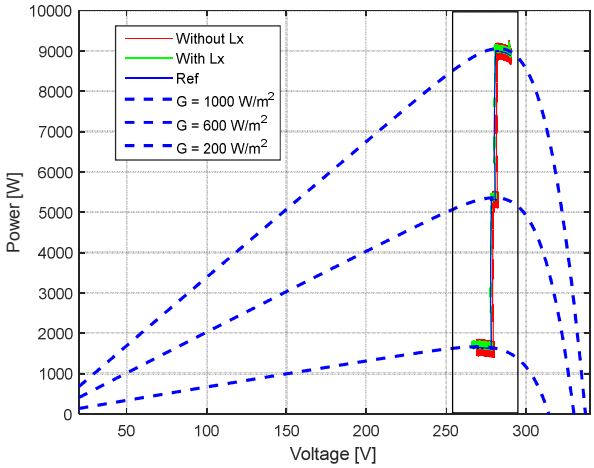
(c)



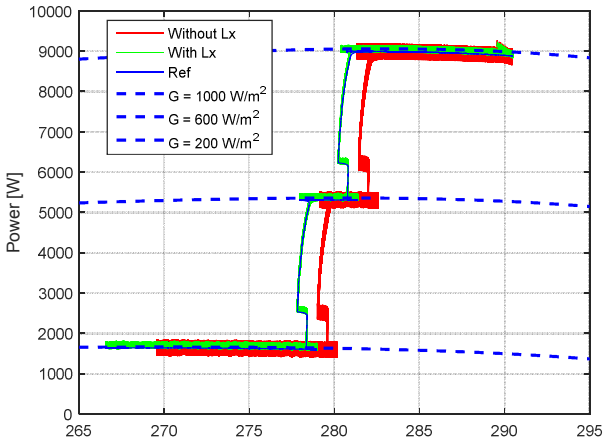
(d)

Fig. 8. Electrical variables of the SAS: (a) Current in the inductor and output current without L_X. (b) Current in the inductor and output current with L_X. (c) SAS output voltage. (d) SAS output power.

Fig. 10 presents the results when the SAS emulates a temperature variation, as presented in case study 2. Fig. 10 (a) and (b) show the currents in the first inductance of the LCL filter and in the second inductance. In a similar way to the previous case, it is observed a reduction in the ripple of the SAS output current with the implementation of the second inductor. Fig. 10 (c) and (d) show respectively the SAS output voltage and the SAS output power.



(a)



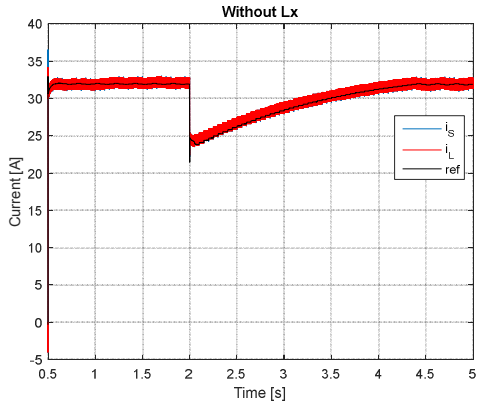
(b)

Fig. 9. (a) Path of the panel emulator during the test of a photovoltaic converter in the P x V plane. (b) Detail of the tracking of the maximum power point.

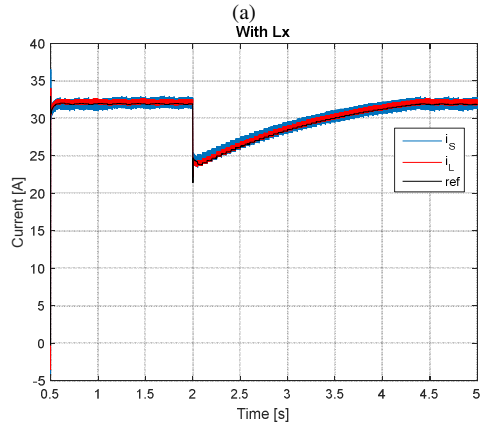
VI. CONCLUSION

The work introduced an alternative topology to emulate a photovoltaic panel. In this topology, an inductive filter is introduced, in order to reduce the output current ripple, allowing to test a wider range of inverters.

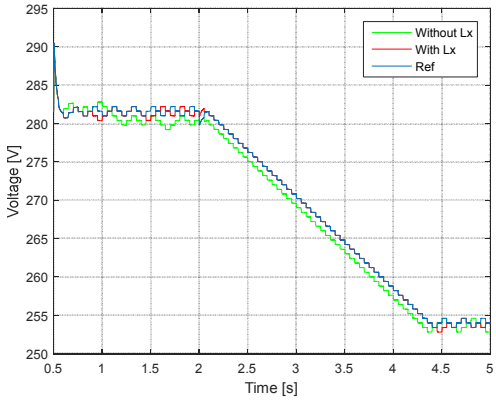
It was observed that the proposed topology presented operational advantages capable of emulating the characteristics of the photovoltaic array and a considerable reduction in the ripple of the SAS output current. The trajectories obtained in the P x V plane also showed the capacity of the inverter to trace the maximum power point of the SAS with smaller oscillations.



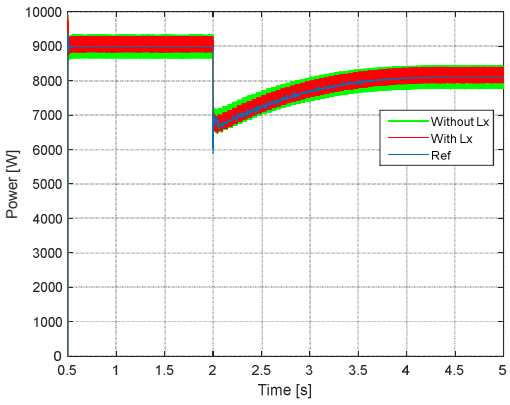
(a)



(b)



(c)



(d)

Fig. 10. Electrical variables of the SAS: (a) Current in the inductor and output current without L_X. (b) Current in the inductor and output current with L_X. (c) SAS output voltage. (d) SAS output power.

ACKNOWLEDGMENT

The authors would like to thank to CNPQ, FAPEMIG and CAPES for their assistance and financial support.

REFERENCES

[1] A. F. Cupertino, V. F. Mendes, G. Y. Santos and E. N. a. P. H. A. Cardoso, Modeling and design of a flexible solar array simulator topology, Minas-Gerais, 2015.

[2] W. B. a. C. Whitaker, Performance Test Protocol for Evaluating Inverters Used in Grid Connected Photovoltaics Systems, Sandia, 2004.

[3] J. Ollila, A medium power PV-array simulator with a robust control strategy, Control Applications, 1995., Proceedings of the 4th IEEE Conference on.1995.p. 40-45, 1995.

[4] H. Matsukawa, K. Koshiishi, H. Koizumi, K. Kurokawa, M. Hamadac and L. Bo, "Dynamic evaluation of maximum power point tracking operation with PV array simulator", Solar Energy Materials & Solar Cells,, Vols. 75, pp. 537-546, 2003

[5] S. Gonzales, Pv array simulator development and validation, Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE. 2010. p.002849{002852. ISSN 0160-8371., 2010.

[6] L. Bun, Development of a real time photovoltaic simulator in normal and abnormal operations., IECON 2011 - 37th Annual Conference onIEEE Industrial Electronics Society. 2011. p. 867-872. ISSN 1553-572X., 2011.

[7] Z. G. Piao, A study on the pv simulator using equivalent circuit model and look-up table hybrid method, Electrical Machines and Systems (ICEMS), 2013 International Conference on. p. 2128-2131, 2013.

[8] M. D. Piazza, Analytical versus neural real-time simulation of a photovoltaic generator based on a dc-dc converter, Vols. 46, n.6, p. 2501-2510. ISSN 0093-9994., Industry Applications, IEEE Transactions on,, 2010.

[9] H. Liu, M. He and X. You, Investigation of photovoltaic array simulators based on different kinds of pwm rectifiers, Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on. 2009. p.737-741, 2009.

[10] S. Ponnaluri, V. Krishnamurthy and V. Kanetkar, Generalized system design and analysis of pwm based power electronic converters, Vols. 3, pp. 1972–1979, Industry Applications Conference, 2000. Conference Record of the 2000 IEEE, 2000.

[11] P. Rodriguez, R. Teodorescu, I. Candela, A. Timbus and M. Liserre, New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions, Power Electronics Specialists Conference, 2006. PESC ’06. 37th IEEE June 2006, pp. 1–7., 2006.

[12] M. Liserre, F. Blaabjerg and S. Hansen, Design and control of an lcl-filter based three-phase active rectifier, Vols. 1, Sept 2001, pp. 299–307, Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE, 2001.

[13] D. Erickson and R. W. M, Fundamentals of Power Electronics, Kluwer Academic Publishers, 2004

[14] D. e. a. Sera, "On the perturb-and-observe and discremental conductance mppt methods for pv sustems.," Photovoltaics, IEEE Journal of, pp. v. 3, n. 3, p.1079-1078, 2013.

[15] M. Villalva, J. Gazoli and E. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays.," Power Electronics, IEEE Transactions on, pp. v.24, n. 5, p. 1198-1208, 2009.