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Capacitor voltage balance performance comparison of MMC-STATCOM using NLC and PS-PWM strategies during negative sequence current injection

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Keywords

Multilevel converters, Static Synchronous Compensator (STATCOM), Modulation strategy, High voltage power converters, Reactive power.

Abstract

This paper addresses the modular multilevel converter applied as a static synchronous compensator. The main objective of this work is to compare the converter performance considering two different submodule capacitor voltage balancing strategies: nearest level control and phase-shifted pulse width modulation, during positive and negative sequence current injection. Results of a 15 MVA MMC STATCOM show that the nearest level control strategy has lower average switching frequency compared to the phase-shifted pulse width modulation strategy, considering comparable submodule capacitance voltage ripple.

Introduction

The modular multilevel converter (MMC) is an emerging power converter technology, which has been considered as a promising solution for high-power voltage source converter (VSC). The main advantages of MMCs are their low switching frequency operation and, at the same time, high number of output voltage level (i.e., low total harmonic distortion), which lead to low semiconductor losses and less filtering requirement. As a consequence, high efficiency operation can be achieved. It can also provide redundancy due to the normally large number of submodules (SMs), which makes it capable of fault tolerant operation. Accordingly, MMCs have been used in several high-power applications commercially, such as high voltage direct current (HVDC) and high-power static synchronous compensator (STATCOM) [1], [2].

Although the MMC offers several advantages (compared to other VSC topologies), its control structure is complex. This is due to the fact that the MMC usually consists of a large number of SMs, which is required for withstanding a high dc-link voltage (in high-power applications) and also for generating a high-level output voltage waveform. In order to ensure a stable operation, the capacitor voltage of all the SMs needs to be balanced [3]. Accordingly, several modulation strategies with their capacitor voltage balancing (CVB) methods have been proposed in the literatures [4]. The performance comparison between different capacitor voltage balancing strategies has also been investigated for HVDC application [5]. However, the performance of different CVB strategies for the STATCOM application has not yet been discussed. Considering the grid connection codes imposed by the transmission system operators, a STATCOM converter has to support the power system by injecting negative sequence current [6]. This negative sequence current injection will, however, affect the variation in the capacitor voltage of the SM in a different way from the MMC HVDC [7]. Specifically, as a consequence of the negative current injection, double frequency power oscillation at AC side occurs. This power oscillation increases the energy variation in the SM capacitors, and thereby challenges performance of the CVB strategies.

Thus, the focus of this paper is on comparing the performance of the CVB strategy employed in the MMC STATCOM. Two most commonly CVB strategies: phase-shifted pulse width modulation (PS-PWM) and nearest level control (NLC) are considered here. The comparison is done by comparing the switching frequency, thermal behavior of the SM, and the power losses of the above two CVB strategies during the positive and the negative sequence injection, while maintaining comparable total harmonic distortion (THD) of the output currents. This paper is organized as followed: the MMC-STATCOM topology and its control are first discussed. The description of the selected CVB strategies is also provided in this section. Then, the thermal model used in losses studies is introduced. The performances of the PS-PWM and the NLC strategies during both positive and negative sequence current injection are examined through simulations. Finally, the conclusion is drawn from the simulation results.

Basic structure and Control scheme of MMC-STATCOM

The system configuration of the MMC-based STATCOM is shown in Fig. 1, referred to as a double-star configuration in the literature [8]. Basically, each phase (also called leg) of MMC consists of a number of SMs connected in series defining an arm structure. The three legs of the MMC are then connected to the common dc-link capacitor C_{dc}. Usually, each SM consists of a half-bridge power module and a SM capacitor C_{sm}. An arm inductor L_{arm} and its internal resistance R_{arm} are used to suppress the high frequency components in the output voltage caused by the SMs switching. Additionally, a small grid-side filter L_g is normally employed, in order to meet the THD requirement of the grid current. The system parameters used in this paper is given in Table I.

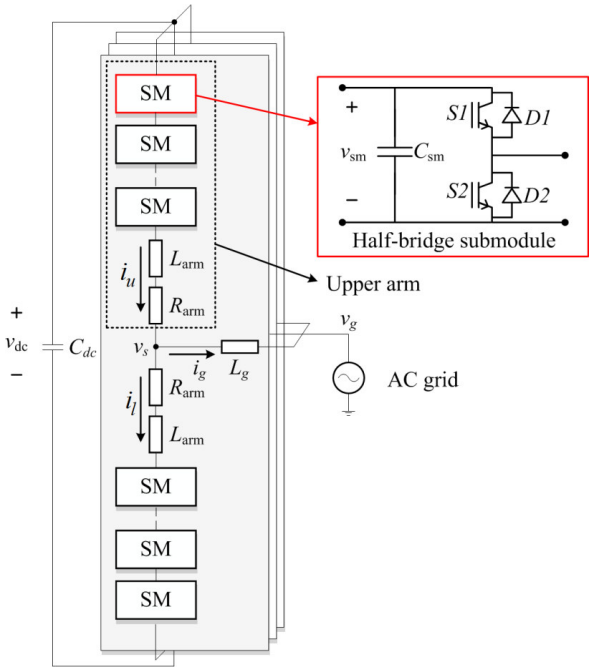

Fig. 1 MMC STATCOM system configuration.

Table I: System Parameters of MMC STATCOM.

Variable	Description	Value
N	Number of SM per arm	20
C_{sm}	SM capacitance (mF)	5.8
C_{dc}	dc-link capacitance (mF)	0.12
L_{arm}	Arm inductor (mH)	28.2
L_g	Grid-side inductor (mH)	1.8
S	Rated power (MVA)	15
V_{SM}	Sub-module voltage (kV)	2.5
f	Grid frequency (Hz)	60
v_g	Grid voltage (kV)	13.8
I_g	Nominal output current (A)	628
I_{SM}	SM rated RMS current (A)	314

The overall control diagram of the MMC STATCOM is illustrated in Fig. 2. At the outer loop controller, the PQ controller is employed in order to control the dc-link voltage (or active power) and reactive power of the STATCOM. This can be achieved by regulating the output current of the MMC, which is done by the inner current control loop. The relation between this two cascaded control loops can be derived as in (1). Then, the reference output voltage of the MMC can be obtained from the current controller. In addition, the so-called circulating current controller, which aims to control the circulating current, is also employed to compensate the circulating current of the converter through the reference output voltage. This circulating current does not contribute to the output current of the MMC, but

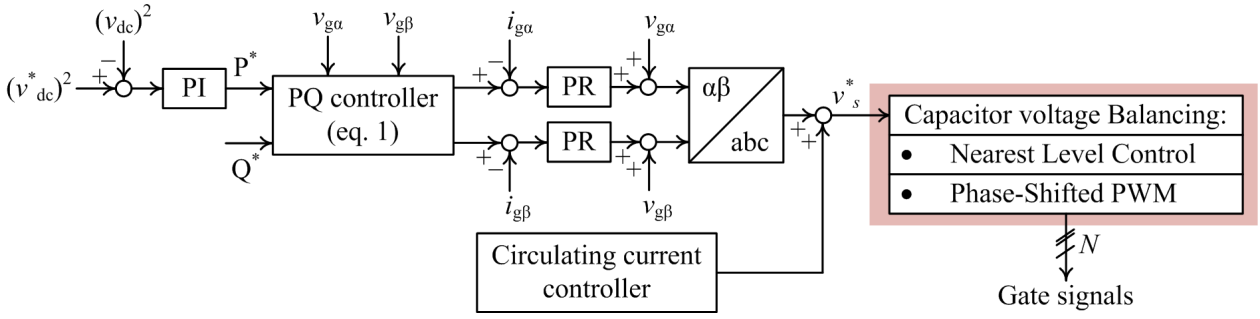

Fig. 2 Overall control diagram of the MMC STATCOM.

circulate among the legs, increasing the conduction losses of the converter, and thus should be suppressed. Then, the output voltage of the converter is produced by inserting and/or bypassing a corresponding number of SM in the arm. In order to ensure a stable operation, the SM capacitor voltages have to be balanced during the operation. This is achieved by the modulation strategy and its capacitor voltage balancing method, which is the main focus of this work. In this section, the two selected capacitor voltage balancing strategies are described.

$$\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} = \frac{1}{(v_{g\alpha})^2 + (v_{g\beta})^2} \begin{bmatrix} v_{g\alpha} & v_{g\beta} \\ v_{g\beta} & -v_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \quad (1)$$

Description of PS-PWM Strategy

The PS-PWM method is one of the most commonly used modulation strategy for MMCs when low number of SM is presented [9]. In this modulation strategy, each SM in the arm has its own carrier wave, which is phase shifted from the other SM carriers. The switching pattern of the SMs is generated by comparing the reference signal n_u with the phase-shifted triangular carrier waves. When the reference amplitude is above the carrier, the corresponding SM to that carrier is inserted to the arm, while the SM is bypassed when the reference is below the carrier. In this way, the gate signal of the SM can be generated, and the switching frequency of the SM is directly determined by the carrier frequency.

Regarding the capacitor voltage balancing strategy, the PS-PWM method requires an extra individual balancing

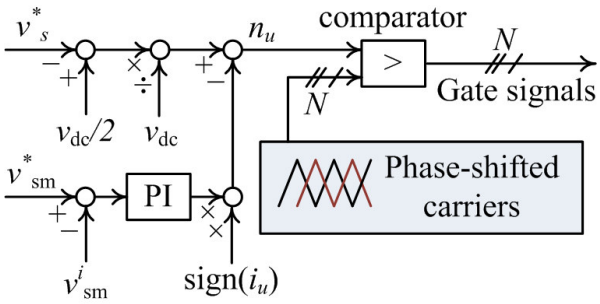

Fig. 3 Control scheme of PS-PWM strategy.

control loop, in order to ensure that the individual capacitor voltage is balanced according to the reference value [10]. The individual balancing controller is basically a simple proportional controller, as it is shown in Fig. 3. Then, its output is multiplied with the arm current direction and added to the reference signal of the modulation.

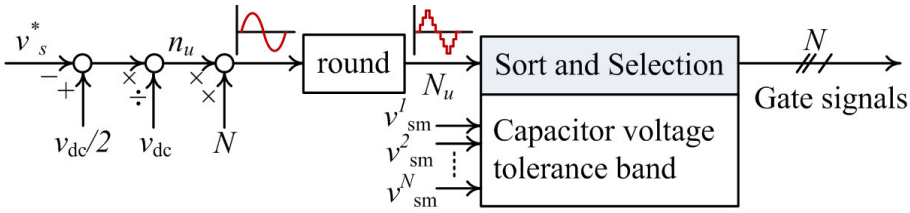

Fig. 4 Control scheme of NLC strategy.

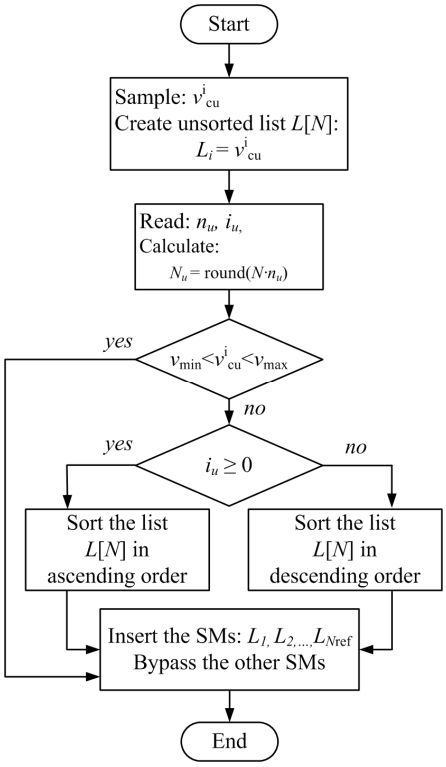

Fig. 5 Flow chart of the NLC with capacitor voltage tolerance band modulation.

Description of Nearest Level Control Strategy

The concept of NLC strategy is to determine the nearest voltage level in each sampling period from the reference output voltage. In order to perform this task, the insertion index n_u is first obtained and scaled with the number of SM in the arm N, at each sampling period. Then, the number of SM to be inserted and/or bypassed needs to be rounded, as the number of the SM in the arm is an integer number. It is obvious that there is always an error between the reference and the generated output voltage due to the rounding process. This error can be reduced by increasing the sampling rate of the NLC algorithm. However, it is noteworthy that there are no carrier waves employed in NLC and the switching frequency of the SM is not directly control, but it is influenced by the sampling frequency of the algorithm.

From the NLC algorithm, the required number of SM to be inserted in the arm is obtained (N_u). Then, in order to ensure the capacitor voltage balance, the NLC strategy requires a sorting and selection algorithm to properly select the SM in the arm to be inserted or bypassed. Basically, the SM capacitor voltage is measured and sorted. Then, during the positive arm current, the SM with the low voltage will be selected to be inserted to be charged, while the SM with high voltage will be bypassed. The action will be opposite during the negative arm current. By doing so, all the SM voltage will be balanced. However, the conventional sorting and selection algorithm proposed in [11] usually

results in a high switching operation. Therefore, a capacitor voltage tolerance band method (CTB) was proposed to improve the performance of the NLC strategy. In general, the sorting and selection is done only when the SM voltage reaches the limit, which is defined as a tolerance band (e.g., 15% of the nominal voltage). The flowchart of the sort algorithm method is illustrated in Fig. 5. Due to its advantage of lower switching operation while maintain the similar output voltage quality with the conventional sorting and selection method, the CTB method will be employed with the NLC strategy in this paper.

Thermal modeling of MMC STATCOM

In order to compare the thermal behavior of the semiconductors in the SM produced by different control strategies, the thermal model of the SM is developed. For the half-bridge SM, the junction temperature of each semiconductor can be estimated by using an equivalent thermal model shown in Fig. 6, where $Z_{th(j-c)}$ is the thermal impedance between the device junction and the case, $Z_{th(c-h)}$ is the thermal impedance between the case and the heatsink, and $Z_{th(h-a)}$ is the thermal impedance between the heatsink and the environment. The thermal model is based on the Foster networks [12], where the model parameters can be obtained from datasheet as it is given in Table II. The analytical formula for the Foster model is given by:

$$Z_{th(jc)} = \sum_{i=1}^{n} R_i(1 - e^{-\frac{t}{T_i}}) \tag{2}$$

where n is the number of RC networks, R_i is the thermal resistance and $T_i = R_i\, C_i$ is the thermal constant of the RC network i. In order to simplify the thermal analysis, a constant heatsink temperature of 60ºC is assumed.

The power losses estimation is based on look-up tables, which is obtained from datasheets. Conduction losses, turn-on and turn-of energy for the IGBT's and the conduction and the reverse recovery energy for the diodes of each SM are considered. Assuming that all the SM and arm parameters are identical, the losses and thermal behavior of all the SM in the arm is similar. Hence, the loss evaluation can be simplified by consider only one arm of the converter.

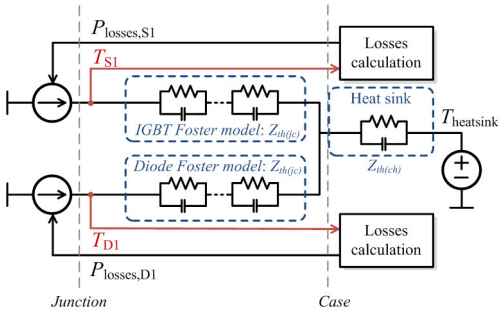

Fig. 6 Thermal model of the half-bridge SM (IGBT and Diode) based on the Foster's network.

Table II: Parameters of the thermal model based on Foster's network [13].

Device	Parameter	$Z_{th(j-c)}$		$Z_{th(c-h)}$
IGBT	R_i (K/W)	0.0128	0.003	0.0012
	T_i (s)	0.151	0.00584	0.1
Diode	R_i (K/W)	0.0255	0.0063	0.0024
	T_i (s)	0.144	0.0058	0.1

STATCOM Operation during Positive and Negative Current Injection

A MMC-STATCOM of 15 MVA connected to a system of 13.8 kV is considered in the simulation, referring to the system configuration as shown in Fig. 2, while the system parameters are given in Table I. Performance of NLC and PS-PWM strategies during the positive and negative sequence current injection are compared in this section.

Positive Sequence Injection

During grid voltage sag, the STATCOM converter needs to inject positive sequence current. This case is simulated considering the STATCOM injecting 1 p.u. of positive current into the grid. The comparison between PS-PWM and NLC strategies is performed considering that both strategies have similar THD in the injected current. For NLC, THD of 0.54% is achieved by selecting the average number of switching (resultant switching frequency) to 120 Hz/SM, as it is shown in Fig. 7(a). This capacitor voltage tolerance band was set to 10% compared to its nominal voltage, as it can be seen in Fig. 8(a). For PS-PWM, higher THD (6.23%) is observed, once it has been obtained by setting the switching frequency to 170 Hz/SM, which results in similar capacitor voltage ripple than NLC strategy, as shown in Fig. 8(b).

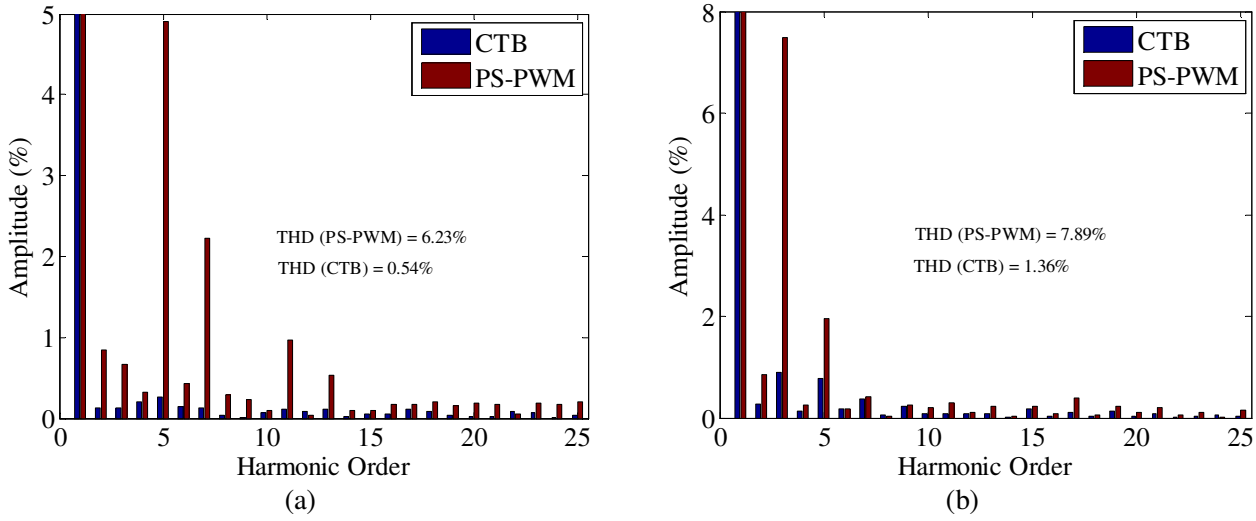

Fig. 7 Grid current THD during 1 p.u. of (a) positive and (b) negative sequence injection.

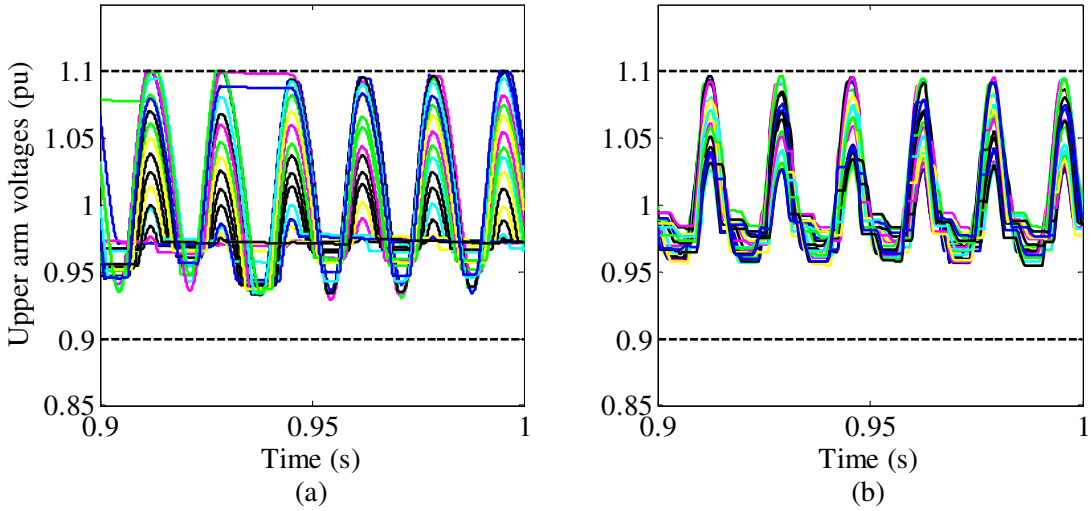

Fig. 8 SM capacitor voltages during positive sequence current injection for (a) NLC and (b) PS-PWM strategy.

Negative Sequence Injection

During asymmetrical fault conditions (e.g., phase to ground faults), STATCOM should also provide negative sequence current. Considering a case when 1 p.u. of negative sequence current has to be injected, the SM capacitor voltage balance performance is analyzed. Fig. 7(b) shows the grid current THD for PS-PWM and NLC strategies. It is observed that the grid current THD is increased in PS-PWM strategy, which is mainly due to an increase in the third harmonic component. However, in terms of average switching frequency for NLC, an increase compared to the positive current injection case is resulted (from 120 Hz/SM to 175 Hz/SM). During negative current injection scenario, the ripple in the SM capacitor voltage becomes larger when NLC strategy is used, as it is shown in the results from Fig. 9(a).

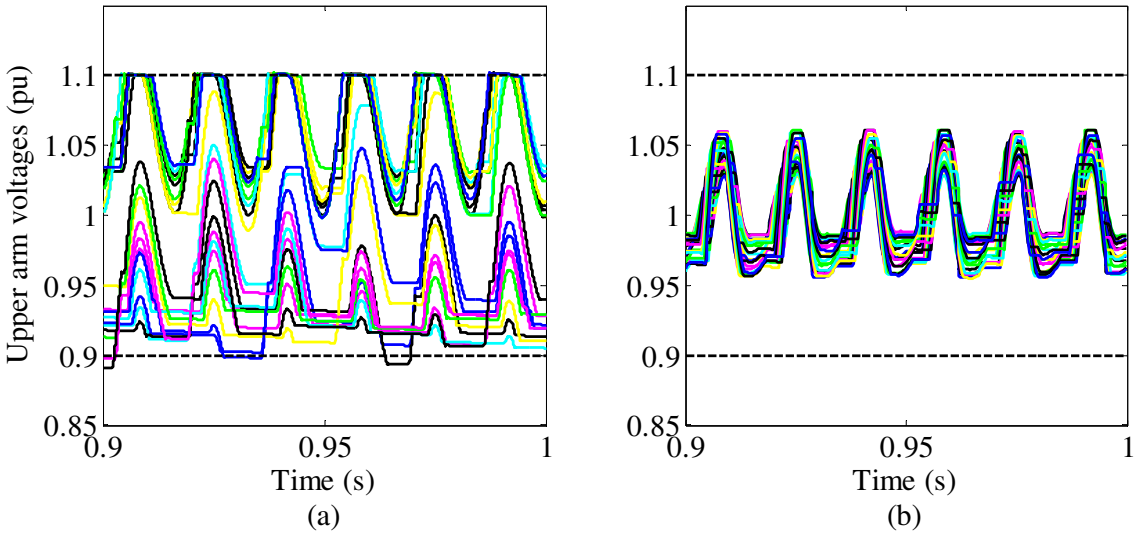

Fig. 9 SM capacitor voltages during negative sequence current injection for (a) NLC and (b) PS-PWM strategy.

Thermal Stress Analysis

In this section, thermal behavior of the devices from the SM is presented. Figs. 10 (a) and (b) show the device junction temperatures for all SMs in the upper arm during 1 p.u. of positive sequence current injection for NLC and PS-PWM strategies, respectively. As a consequence of lower switching frequency using NLC strategy, the device junction temperature is around 20°C lower when compared to the PS-PWM

The lower device junction temperature with the NLC strategy is also observed during 1 p.u. of negative sequence current injection, as it is shown in Fig. 11. However, in the case of PS-PWM strategy, the junction temperatures of the upper diode D1 during the negative sequence current injection is around 10°C higher than the positive sequence current injection case. Fig. 12 shows the conduction and switching losses in the SM from both strategies. The low switching frequency in NLC results in lower switching losses, compared to the PS-PWM.

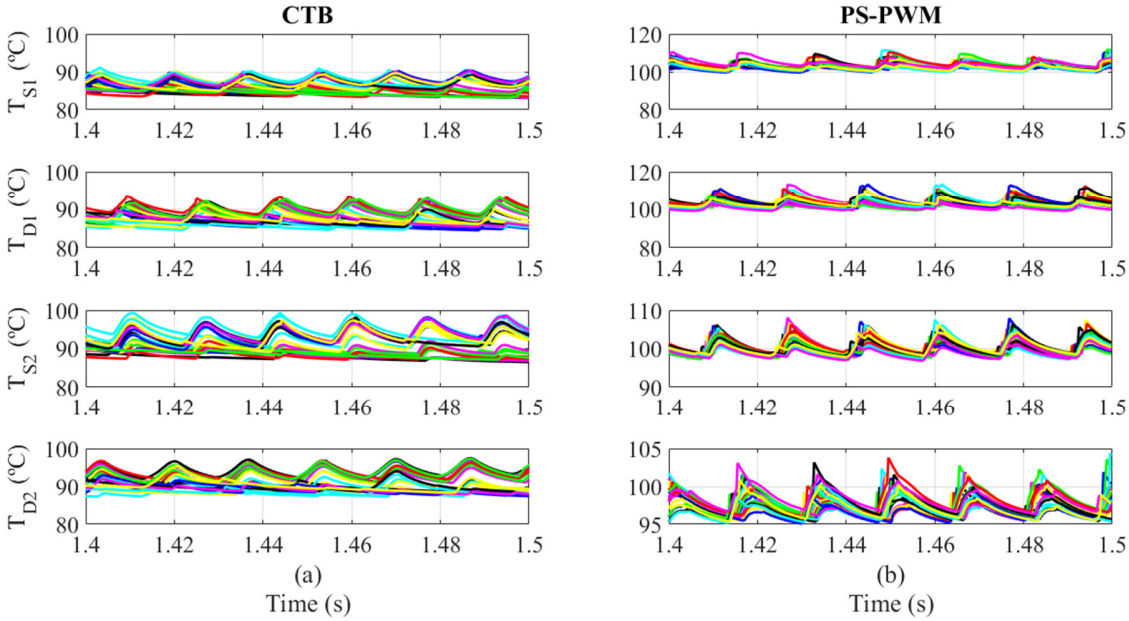

Fig. 10 Devices temperatures in the SM during positive sequence current injection in (a) NLC and (b) PS-PWM strategies.

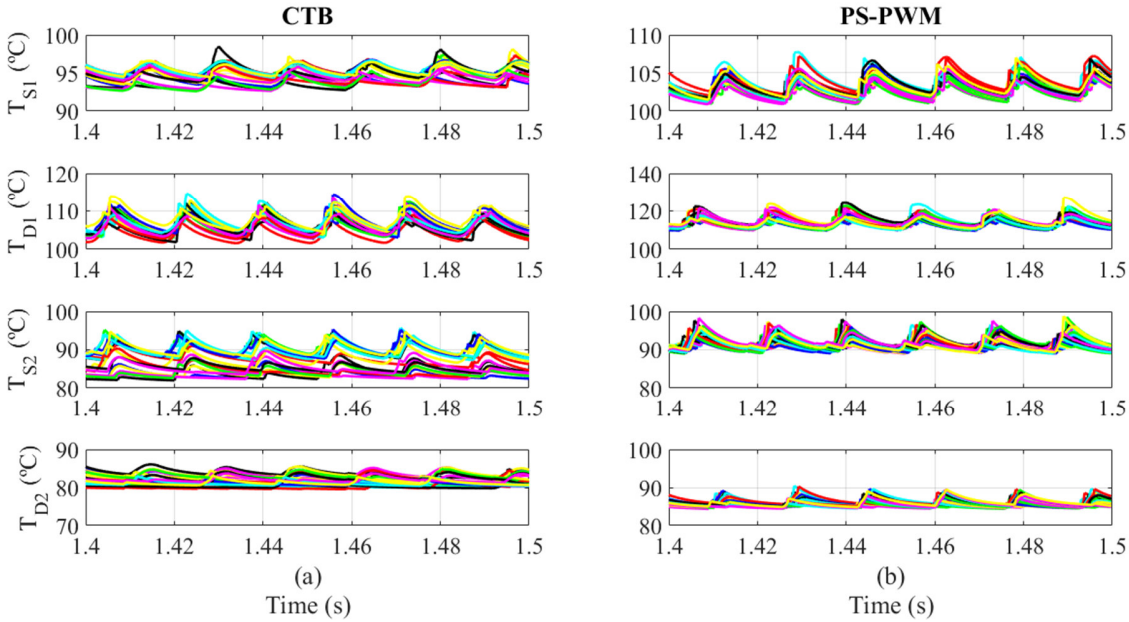

Fig. 11 Devices temperatures in the SM during negative sequence current injection in (a) NLC and (b) PS-PWM strategies.

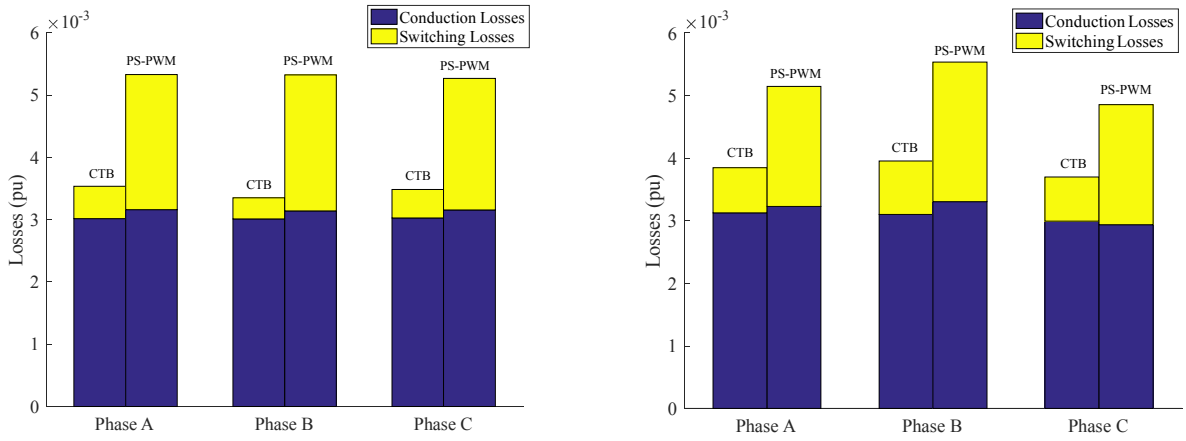

Fig. 12 Conduction and switching losses distribution during 1 p.u. of (a) positive and (b) negative sequence current injection for NLC-CTB and PS-PWM strategies.

Conclusion

This work compares two methods to modulate and balancing the submodule capacitor voltages in a double-star MMC-based STATCOM converter. During positive and negative sequence current injection, NLC strategy presents similarities with PS-PWM strategies in terms of submodule capacitance voltage ripple. However, NLC strategy can operate with lower switching frequency, while still maintaining the capacitor voltage to be balanced. Thus, the switching loss in the NLC strategy is lower than that in the PS-PWM method. Consequently, lower device junction temperature is achieved with the NLC strategy during both positive and negative current injection.

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